P/N 4411-0006

ST-130
and
ST-135
Controller

Operation manual

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Chapter 1
Description

The Model ST-130 and ST-135 Camera Controllers offer many sophisticated hardware features. Designed for precision image acquisition, they offer A/D converters with as much as 18 bits of dynamic range. The two models differ primarily in the way they interface to the system computer. Both serial and parallel interfaces are available for the ST-130. The ST-135 on the other hand communicates with the computer via an IEEE-488 GPIB Interface. *See Appendices C and D for information regarding the GPIB software configuration and required internal switch settings.*

ST-130 and ST-135 Features

This camera controller has many unique features, available only from RS Princeton Instruments. Hardware features of the ST-130 include:

- Up to 16 bits/pixel A/D range, 18 bits with binning
- Complete system readout noise of 1-1.3 A/D counts RMS
- Linearity
- Full resolution image readout
- Flexible subimaging
- On-chip charge binning of rectangular regions of pixels
- Patterned skipping of unimportant image areas for increased frame rates
- High speed dark current cleaning, < 1 msec/frame on some CCDs
- Sophisticated triggering and synchronization
- High speed burst DMA data transfer to memory on IBM/AT or Macintosh computers
- Temperature regulation for thermo-electrically or liquid nitrogen cooled cameras to ±0.050°C.
- Support for CCD camera formats from 576 x 384 to 3,072 x 2,048
- Support for MPP operation
- All PI ICCD and ITE cameras, 18 or 25 mm intensifiers
- Auxiliary digital and analog I/O, for complete experiment integration, all under software control

A/D Converters and Architecture

It is often desirable to optimize the signal from a CCD camera by changing the digitization rate. Higher speeds may be required for rapid image collection, while a slower speed minimizes readout noise, increasing the overall dynamic range. A/D converter speed and precision describe the A/D converter only. Overall system performance depends on the capabilities of the camera as well.

Cameras Supported

Most RS Princeton Instruments CCD cameras can be operated by the Model ST-130 Camera Controller. All of these CCD cameras can be operated at 150 kHz. Other Controllers such as the Model ST-138 and ST-133 are available for operating at higher speeds.

RS Princeton Instruments also offers fiber or lens coupled intensified CCD cameras based on many of these arrays.

Temperature Control

The ST-130 Controller provides power and control for thermoelectric cooling of PI CCD detectors. Front panel LEDs indicate when the temperature is fully regulated. Regulation is also provided for liquid nitrogen cooled detectors, to maintain an operating temperature between -70 and -140°C. Precise removal of dark charge signal is a key factor in many low light applications. To be able to subtract dark charge precisely, its level must not fluctuate between the measurement of the dark charge level and the measurement of the image. Because the dark current of most CCD arrays is an exponential function of temperature, doubling roughly every 4-7°C, precision temperature regulation is crucial. The ST-130 Controller regulates the temperature of the CCD array to ±0.050°C over the full operating temperature range. This translates into dark current stability of ±½% or better on most CCD arrays.

Timing Modes

The ST-130 has several built-in timing modes, for experiment synchronization. Both trigger in and trigger out TTL signals are available, for maximum flexibility. The Model ST-130 supports the following timing modes.

Freerun

In this mode, the camera continuously collects images. The controller will continue to read out frames until the software instructs it to stop. The Model ST-130 and ST-135 Camera Controllers offer many standard features for collection of high dynamic range images.

External Sync

This mode is similar to Freerun except that each time the camera is ready to begin an exposure, it waits to receive an external signal. Once this signal is received, the system waits for the duration of the preset exposure time, closes the shutter, and reads out the CCD. The shutter can be opened before or after the external pulse. Store-Enable Triggering Along with the above timing options, a second trigger input can be used to determine whether data is to be stored. This allows a camera to be run continuously, storing frames asynchronously, i.e., only when an event has occurred during a read-out/ exposure cycle.

On-Chip Charge Binning Control

During each frame digitizing cycle, each row of the CCD is shifted “vertically” into the serial shift register of the CCD. If another row has previously been shifted into the serial shift register and not read out, then the charge of the new line will be automatically combined with the charge already there. This is called row binning. With the ST-130 Controller, as few as one or as many as all rows can be binned together. In addition, unwanted data can be read without digitizing. This “skipping” is much faster than readout with digitizing. Once the correct number of rows have been shifted in parallel into the serial register of the CCD, the register is read out. This is done by clocking the serial register once for each pixel. As the charge in a given pixel is shifted out the end of the serial register, it enters a charge detecting capacitor. Here it can either be skipped, digitized, or binned.

Readout Mode Options

- The flexible programming of the ST-130 allows the following common readout modes:
- Readout and digitization of the whole array at full resolution.
- Readout and digitization of a rectangular subsection of the array at full resolution. This results in a higher readout rate and is useful for focusing.
- Readout with N x M binning. This reduces resolution but increases the readout rate. Because N x M binning combines the charges from many pixels, the apparent sensitivity of the camera is increased, allowing shorter exposure times to be used.
- Readout and digitization of rectangular bands of pixels, binned to give a one dimensional output. This mode of readout offers fast cross section readouts.
- Readout with patterned row and column skipping. This allows the whole CCD or any part of it to be read out with lower resolution, but without binning.

Computer Interface

The ST-130 Controller has a high speed burst mode DMA interface that can sustain data transfers to IBM AT compatible computers at 300 kilopixels/second. Use of DMA means that the amount of data that can be taken is limited only by the memory capacity

of the computer. The data is also immediately accessible to the microprocessor for real time display or analysis. Now standard, an optional high speed serial interface has been developed for use with AT, Macintosh, and other computers. This interface allows separation of the controller and the computer up to 50 m. A fiber optic link increases this distance to 2 km.

The Model ST-135 Camera Controller uses a GPIB standard interface for communicating with a number of different computer platforms. Maximum data transfer rates are 400 kbytes per second. Not all computers that claim to be 100% IBM AT compatible actually are. RS Princeton Instruments maintains a list of computers that have been verified for operation with its equipment. Consult your sales representative for specifics.

Peripheral I/O

Synchronization and/or control signals

- External sync input: TTL low; up to (1/ t_{frame}) Hz
- External shutter control input: TTL low to open
- Trigger output: TTL low at the start of data acquisition
- Notscan output: TTL high during exposure, low during readout
- Frame, line, and pixel clocks: TTL outputs
- Shutter drive monitor: TTL output, high during active shutter drive
- I/O inputs: 8 TTL lines
- Digital outputs: 8 TTL output, 4 inverted, 4 high voltage capable (60 V, 0.5 A switches)
- Analog input (optional): One input, 0 to +10 V used for normalization, e.g., for light source variation.

Software

Several software packages are available for operating RS Princeton Instruments equipment, depending on the type of experiment you are running. Spectroscopic data is collected using WinSpec/32 . The software package for imaging is WinView/32. *16 bit versions of WinSpec and WinView that run under Windows 3.1 continue to be available.* Each of these packages are complete systems, and each has specific hardware and software requirements. Other software packages are available that operate this controller via Macintosh computers. For detailed instructions on installing and operating any of these software packages, see the manual provided with your particular software.

Chapter 2
Controller Setup

Introduction

This chapter explains the initial steps in setting up your controller. It will take you step by step through procedures for safe operation of your ST-130 or ST-135.

Unpacking the Controller

During unpacking, check the system for possible signs of shipping damage. If there is any, notify RS Princeton Instruments and file a claim with the carrier. If damage is not apparent but system specifications cannot be achieved, internal damage has probably occurred.

Equipment and Parts Inventory

The complete system is composed of a computer, an ST-130 or ST-135 Controller, a TE/CCD, LN/CCD, or ICCD series detector, and a gate pulser (optional). Also included are the following:

Detector to controller cable: 6 ft. standard. Lengths up to 20 feet with RF shielding are available.

ST-130 only: 25 ft. standard serial or 6 ft. parallel controller to computer cable. Serial lengths up to 165 feet are available. Optional fiber optic transducers can be used with standard controllers and detectors, extending this distance up to 2 km.

ST-130 only: High Speed Serial Buffer Board or Parallel Buffer Board (to be installed in the computer by the user, if not installed at the factory).

Precautions

The apparatus described in this manual is of Class I category as defined in IEC Publication 348 (Safety Requirements for Electronic Measuring Apparatus). It is designed for indoor operation only. Before turning on the controller, the ground prong of the power cord plug must be properly connected to the ground connector of the wall outlet. The wall outlet must have a third prong, or must be properly connected to an adapter that complies with these safety requirements.

WARNING

If equipment is damaged, the protective grounding could be disconnected. Do *not* use damaged equipment until safety has been verified by authorized personnel. Disconnecting the protective earth terminal, inside or outside the apparatus, or any tampering with its operation is also prohibited.

Inspect the supplied power cord. If it is not compatible with the power socket, replace the cord with one that has suitable connectors on both ends.

WARNING

Replacement power cords or power plugs must have the same polarity as that of the original ones to avoid hazard due to electrical shock.

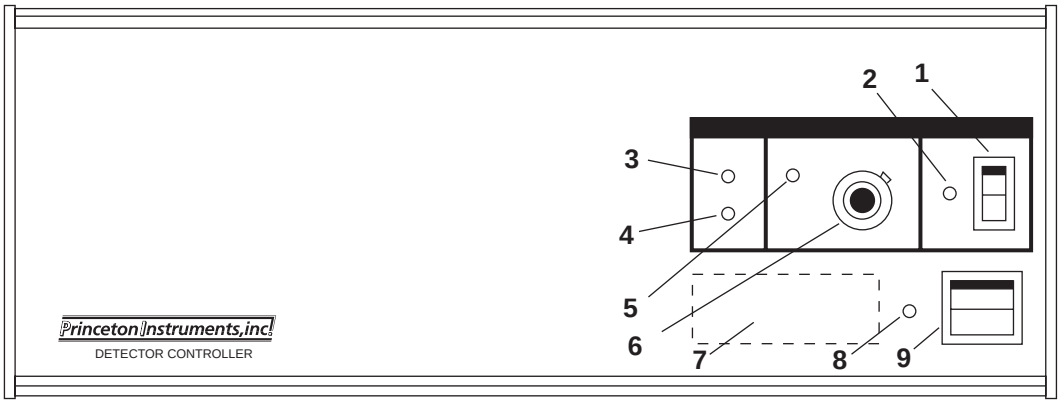


Figure 1. ST-130 and ST-135 front panel

Front panel functions

1. Cooler power switch
2. Cooler power indicator (yellow)
3. Cooler status (yellow) indicates that the detector is not yet thermostated
4. Cooler status (green) indicates that the detector is thermostated to within ±0.05°C of the set temperature
5. Warning indicator (red) if temperature is set too low
6. Temperature setting potentiometer, calibrated in minus °C
7. GPIB indicator panel (ST-135 only)
8. Power on indicator (yellow)
9. Controller power switch

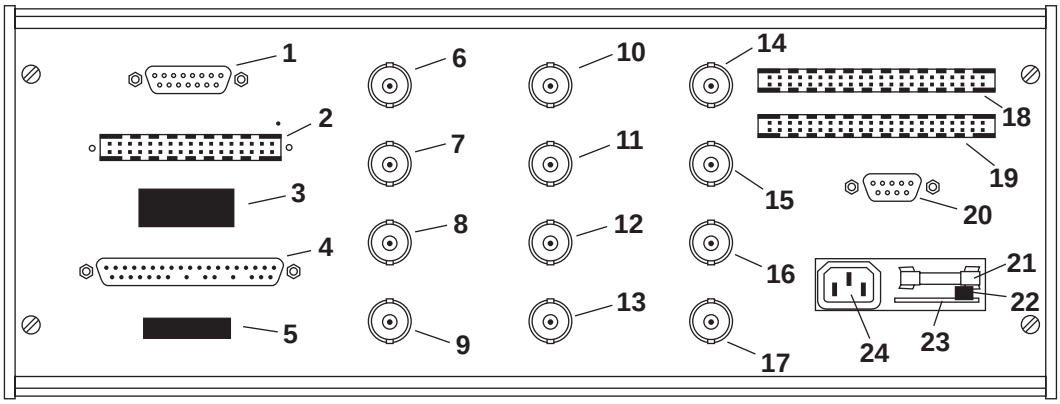


Figure 2. ST-130 rear panel

Rear panel functions

	Label	Function
1.	J6	Digital sync for frame grabber board
2.	J5	Auxiliary port (34 pin), 8 bit software programmable digital I/O port, see Appendix E for details
3.	IEEE-488	GPIB-488 parallel port (ST-135 only)
4.	DETECTOR	Detector head cable connector: DB-37-M
5.	RS-232	Serial port for communicating via RS232C
6.	CRT X	X-ramp signal for multisync monitor
7.	TRIGGER OUT	TTL low (negative edge) during data acquisition
8.	NORMALIZE 1	0-10 V signal for source compensation
9.	NORMALIZE 2	Shutter monitor (optional)
10.	CRT Y	Video out monitor: 0-10 V
11.	TRIGGER IN	External trigger input: TTL low level activated
12.	NOTSCAN	TTL low when sensor is being read; TTL high indicates sensor currently being exposed
13.	NORMALIZE 3	Not used
14.	CRT Z	Negative blanking signals for XYZ monitor
15.	EXT SYNC	External sync input: TTL low level activated
16.	SHUTTER	External shutter control; TTL level; TTL low forces shutter open. In certain timing modes, complete control of shutter is possible. *Not provided on ST-130.*
17.	NORM 4/VIDEO	0-1.3 V normalized video out for frame grabber board
18.	J3	Connector for communicating via DMA with Buffer Board inside computer (parallel ST-130 only)

19.	J4	Connector for communicating via DMA with Buffer Board inside computer (parallel ST-130 only)
20.	J7	Connector for communicating with Serial Buffer Board inside computer (serial ST-130 only)
21.		Fuse
22.		Fuse release lever
23.		Voltage selector card
24.		AC power cord slot

Internal settings of the controller appear in Appendix B. Except in cases where multiple equipment is present, the factory settings should not be reset by the user.

Setting the Line Voltage

Prior to operation, the voltage selector card on the controller must be set to match the line voltage of the wall outlet. This setting is either 100, 120, 220, or 240 V, at either 50 or 60 Hz. An incorrect setting may result in damage to the apparatus.

To check the voltage setting, read the number appearing on the top surface of the card, directly below the fuse. To change the setting, turn off the controller, remove the power cord, and slide the clear plastic fuse cover to the left. Next move the fuse release lever (lower right) to the left, until the fuse is ejected. Pull out the setting card and reinsert it with the correct number showing.

Check that the fuse provided matches the line voltage according to the table below. If so, put the fuse back in place, slide the cover to the right, and reinsert the power cord.

Table 1. Voltage and fuse selection.

Voltage	Fuse
100-120 V*	2 A slow blow
220-240 V	1 A slow blow

*With an 18 bit A/D, the ST-130 and ST-135 will not operate properly from 100 V line voltage. 120 V, 220 V and 240 V are all available and do work correctly.

Turning on

Connect the power cord to the controller and the wall outlet. Before turning on the controller, check that the cooler switch is in the OFF position. The controller may now be turned on.

Note: A brief alarm (2 seconds or less) may sound when the system is first turned on. This alarm is used with intensified detectors (ICCDs), and will continuously sound when there is too much incident light on the intensifier. If the alarm sounds continuously, immediately lower the light level and/or power down the system.

With the cooler switch off, the yellow status light should be lit, as well as the yellow power light. Before proceeding to the next step, turn the power switch OFF.

Chapter 3
Installing the Buffer Board

This chapter will lead you through the process of installing the PCI Serial, ISA Serial, EISA Serial, NuBus Serial, or ISA Parallel Buffer Board. Following these steps explicitly will help insure proper connection to your computer.

CAUTION

For computers with an EISA bus only, special configuration software must be run, sometimes before the card is installed. Read the documentation that came with your computer before attempting to install the serial buffer board.

A screwdriver may be needed to remove screws from the computer (the type varies from computer to computer). A small, flat-bladed screwdriver is needed to connect both ends of the serial cable.

PCI Serial Buffer Board

Introduction

If the computer is a PCI bus PC, it must be equipped with an PCI Serial Buffer board. Information about the installation and operation of this board follows.

CAUTION

A PCI Serial board must be installed in an x86 type computer having a motherboard with at least one free PCI slot. The PCI Serial card must be plugged into a PCI slot. If using WinView/32 or WinSpec/32 software, **High Speed PCI** must be the selected Interface type. *Note that the displayed I/O Address and Interrupt Level values do not reflect the actual settings negotiated by the card and bus at startup. These parameters are determined automatically for the PCI card.*

A screwdriver may be needed to remove screws from the computer (the type varies from computer to computer). A small, flat-bladed screwdriver is needed to connect both ends of the serial cable.

Installing the PCI Card

- Remove the expansion slot cover on the rear panel of the I/O slot selected (see Figure 4).
- Insert the PCI Serial Interface card as far as possible into the appropriate PCI socket (see Figure 5). Then secure the Serial Buffer Board by reinstalling the expansion slot cover screw.

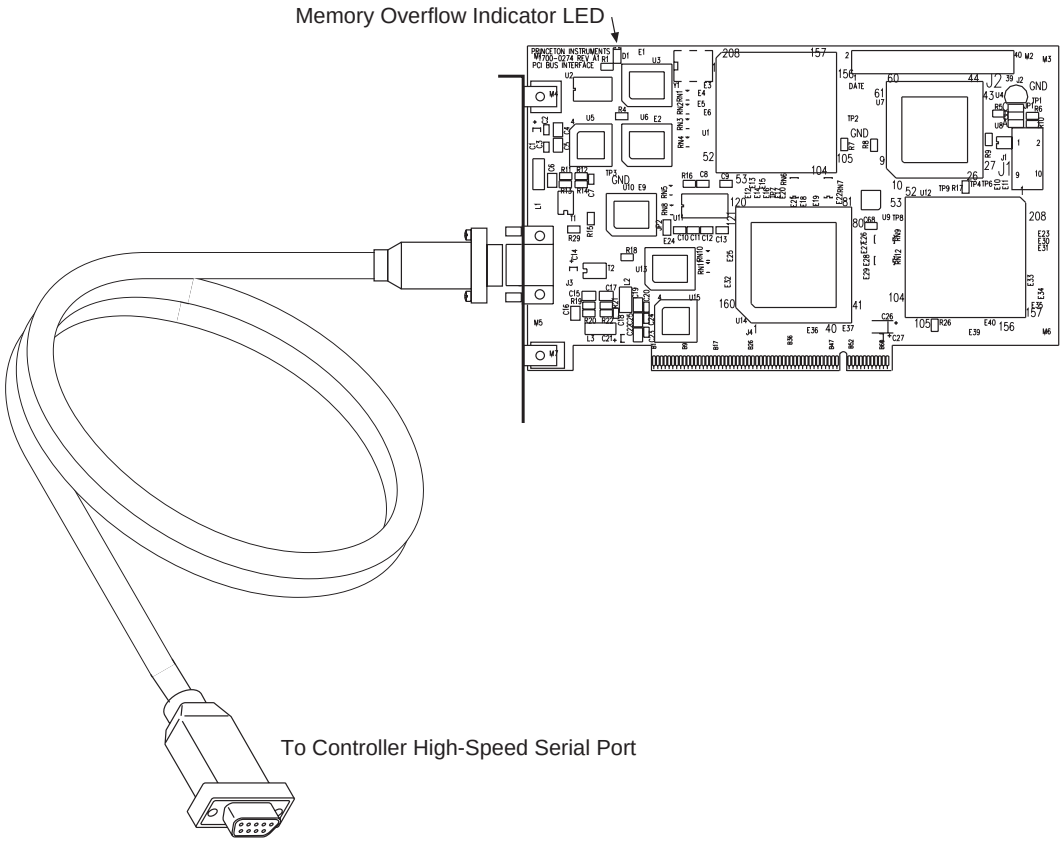


Figure 3. PCI serial board

Connect the standard TAXI* serial cable to the nine-pin cable connector on the PCI Serial Buffer Board mounting panel as shown in Figure 3. The other end of the serial cable connects to the Controller's high-speed serial output connector (item 20 in Figure 2). Take care to tighten the screws at both ends of the cable using a small, flat-bladed screwdriver.

Virtual Device Driver Installation

For the PCI card to operate, the virtual device driver PIPCI.386 must be installed in the computer. When operating under Windows 3.1, this driver file can be placed in either of two places, the **\windows** directory or the **\windows\system** directory. WinView 1.6 loads PIPCI.386 automatically when it is installed. If the PCI card is being installed at PI, the driver will be loaded as part of the installation. If the PCI card is not being installed at the factory, it will be necessary to obtain a copy of PIPCI.386 (available from the factory) and install it manually, or to install WinView *(ver 1.6 or higher)* so that PIPCI.386 will be installed automatically.

Note: Do not install pipci.386 manually if using WinView/32 or WinSpec/32. Instead, repeat the installation (custom) and select PCI as the interface to automatically load any required PCI drivers.

* TAXI is a registered trademark of AMD Corporation.

If PIPCI.386 is installed manually, it will be necessary to edit the **system.ini** file, which is located in the **windows** directory. Using an ASCII editor, such as DOS Edit, add the following line to the **[386Enh]** section of **system.ini**.

device=pipci.386

The precise location within the **[386Enh]** section of **system.ini** isn't important. For example, the edited file might appear as follows.

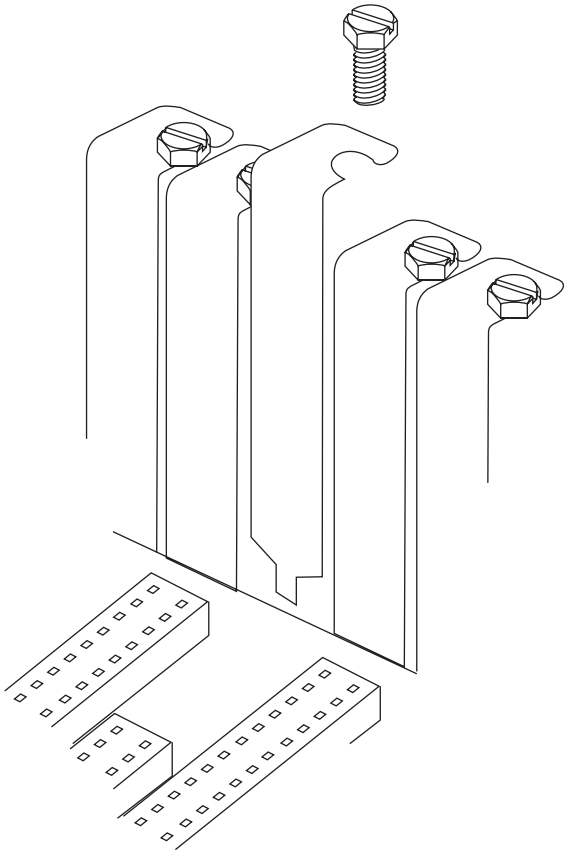
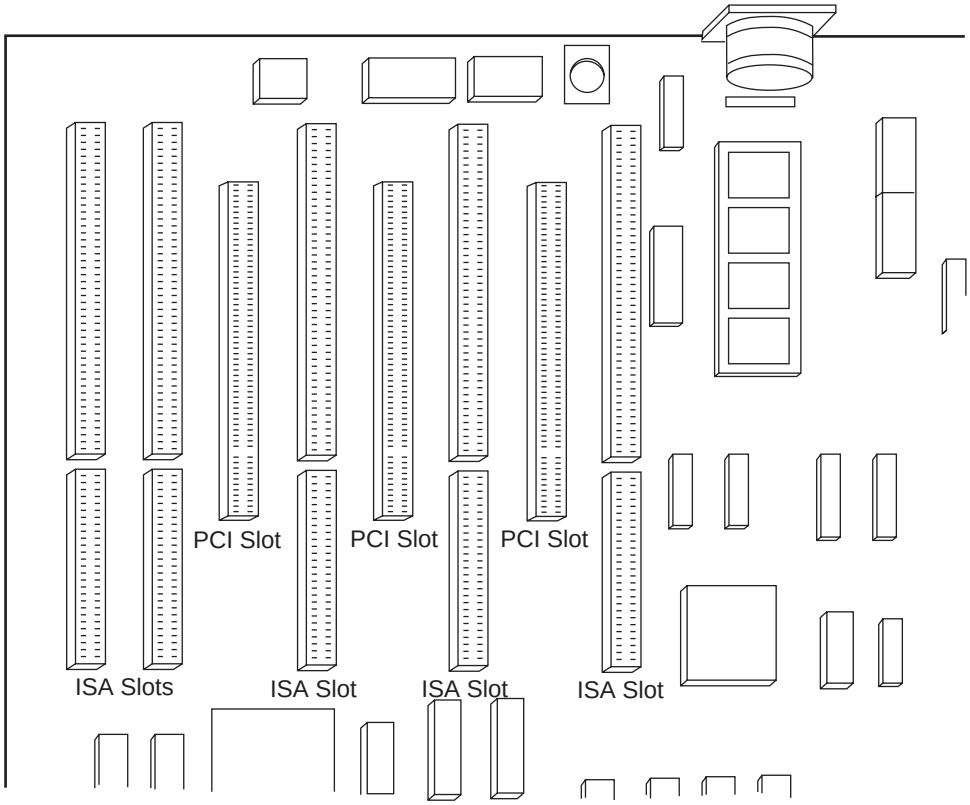


Figure 4. Removing the expansion slot cover on an AT type computer

Figure 5. PCI expansion slots in typical computer




```
[386Enh]
display=vdds3764.386
device=v3152d.386
DMABufferSize=384
device=*vmcpd
WinExclusive=0
device=pipci.386
…..
…..
```

CAUTION

If “device=pipci.386” should appear more than once in the system.ini file, an error condition will be generated when the computer boots. To correct the condition it will be necessary to use an ASCII editor to remove one of the device= pipci.386 statements.

Power-On Checks

Introduction

Before proceeding, be sure the Serial Buffer Board is firmly mounted in the slot. Replace the cover of the computer and turn on the computer only. If an error occurs at bootup, either the PCI serial card was not installed properly or there is an address or interrupt conflict.

Conflicts

One of the many advantages that PCI offers over ISA is that the whole issue of address and interrupt assignments is user transparent and under BIOS control. As a result, users typically do not have to be concerned about jumpers or switches when installing a PCI

card. Nothing more should be required than to plug in the card, make the connections, and operate the system. As it turns out, however, in certain situations conflicts may nevertheless occur and user intervention will be required to resolve them.

Typical PCI motherboards have both ISA and PCI slots and will have both PCI and ISA cards installed. In the case of the ISA cards, the I/O address and Interrupt assignments will have been made by the user and the BIOS will not know which addresses and interrupts have been user assigned. When a PCI card is installed, the BIOS checks for available addresses and interrupt levels and automatically assigns them so that there are no *PCI* address or interrupt conflicts. However, because the BIOS doesn't know about the user-assigned ISA I/O address and interrupt level assignments, it is possible that a PCI card will be assigned an address or interrupt that is already assigned to an ISA card. If this happens, improper operation will result. Specifically, the problems could range from erratic operation under specific conditions to complete system failure. If such a conflict occurs, because the user has no control over the PCI address and interrupt assignments, there will be no recourse but to examine the ISA assignments and change them to values which do not conflict. Most (but by no means all) ISA cards make provision for selecting alternative I/O addresses and interrupt levels so that conflicts can be resolved. Software is available to help identify specific conflicts.

The following example may serve to illustrate the problem. Suppose you had a system with an ISA network card, a PCI video card and an ISA sound card. Further suppose that you were then going to install a PCI Serial Buffer card. Before installing the PCI Serial card, the I/O address and interrupt assignments for the installed cards might be as follows.

I/O Address & Interrupt Assignments
Before Installing Serial Card

Slot Type	Status	I/O Address	Interrupt
1 (ISA)	ISA Network Card	200-210	11
2 (PCI)	PCI Video Card	FF00-FFFF	15
3 (ISA)	ISA Sound Card	300-304	9
4 (PCI)	Empty	N/A	N/A

As shown, there are no conflicts, allowing the three peripheral cards to operate properly. If the PCI Serial card were then installed, the BIOS would interrogate the PCI cards and may reassign them new address and interrupt values as follows.

I/O Address & Interrupt Assignments
After Installing Serial Card

Slot Type	Status	I/O Address(s)	Interrupt
1 (ISA)	ISA Network Card	200-210	11
2 (PCI)	PCI Video Card	FE00-FEFF	11
3 (ISA)	ISA Sound Card	300-304	9
4 (PCI)	PI PCI Serial Card	FF80-FFFF	15

As indicated, there is now an interrupt conflict between the ISA Network Card and the PCI Video card (both cards have been assigned Interrupt 11), causing the computer to no longer function normally. This doesn't mean that the PCI Serial card is defective because the computer stops functioning properly when the Serial card is installed. What it does mean is that there is an interrupt conflict that can be resolved by changing the interrupt level on the conflicting Network card in this example. It is up to the user to consult the documentation for any ISA cards to determine how to make the necessary change.

Note: Changing the order of the PCI cards, that is, plugging them into different slots, could change the address and interrupt assignments and possibly resolve the conflict. However, this would be a trial and error process with no guarantee of success.

Diagnostics Software

Many diagnostics programs, both shareware and commercial, are available to help resolve conflicts. Most often, all that's required is a program that will read and report the address and interrupt assignments for each PCI device in the computer. One such program available from PI's Technical Support department is called PCICHECK. When the program is run, it reports the address and interrupt assignments for the first PCI device it finds. Each time the spacebar is pressed, it moves on to the next one and reports the address and interrupt assignments for that one as well. In a few moments this information can be obtained for every PCI device in the computer. Note that, even though there are generally only three PCI slots, the number of PCI devices reported may be larger because some PCI devices may be built onto the motherboard. A good strategy for using the program would be to run it before installing the PCI Serial card. Then run it again after installing the card and note any address or interrupt assignments that may have changed. This will allow you to easily focus on the ones that may be in conflict with address or interrupt assignments on ISA cards. It might be noted that there are many programs, such as the MSD program supplied by Microsoft, that are designed to read and report address and interrupt assignments, including those on ISA cards. Many users have had mixed results at best using these programs.

Operation

There are no operating considerations that are unique to the PCI Serial card. The card can easily accept data as fast as any PI System now available can send it. The incoming data is temporarily stored in the card’s memory, and then transferred to the main computer memory when the card gains access to the bus. The PCI bus arbitration scheme assures that, as long as every PCI card conforms to the PCI guidelines, the on-board memory will never overflow.

Unfortunately, there are some PCI peripheral cards that do ***not*** fully conform to the PCI guidelines and that take control of the bus for longer periods than the PCI specification allows. Certain video cards (particularly those that use the S3 video chip) are notorious in this respect. Usually you will be able to recognize when memory overflow occurs because the displayed video will assume a split-screen appearance. At the same time, the LED on the upper edge of the PCI Serial card will light.

Users are thus advised not to take any actions that would worsen the possibility of memory overflow occurring when taking data. In that regard, avoid multitasking while taking data. Specific operations to avoid include multitasking or running a screensaver program.

ISA Serial Buffer Board

Introduction

An ISA Serial board must be installed in an "AT type" computer to communicate with the Controller and can be plugged into either an ISA slot or an EISA slot. If plugged into an EISA slot, you must select "High Speed Type B" as the board type via the WinView or WinView/32 software.

Installation Steps

CAUTION

Do ***not*** attempt the EISA configuration if installing an ISA Serial card installed in an EISA slot. Not only is it unnecessary to perform an EISA configuration, but attempting to do it could seriously alter the computer's normal functioning.

A screwdriver may be needed to remove screws from the computer (the type varies from computer to computer). A small, flat-bladed screwdriver will additionally be needed to tighten the screws that secure both ends of the serial cable.

Note: EISA and ISA bus connectors are superficially similar, making it possible to mistake an ISA bus computer for an EISA bus computer. Two ways of telling whether the bus is EISA or ISA are by the bus connectors' color and by the number of contacts.

- EISA bus connectors are ***brown***. ISA bus connectors are ***black***.
- ISA bus connectors have either 31 or 49 contacts. The contacts in an EISA bus connector are arranged in two levels, upper and lower. On the upper level are the same 49 contacts as are present on a full-length ISA bus card. On the lower level is a second set of 45 contacts which are only present on EISA bus connectors. However, the location of the lower contacts makes them difficult to see.

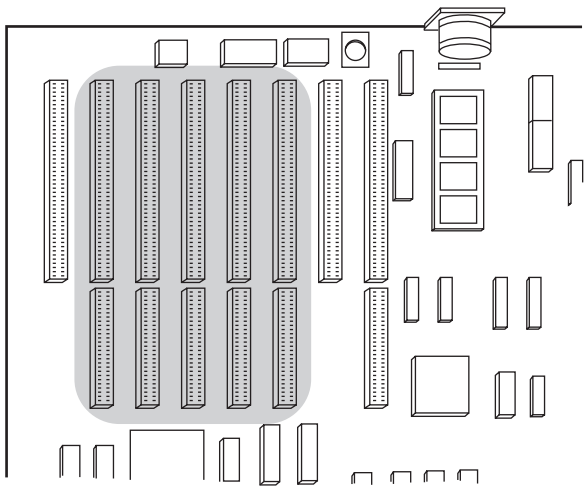
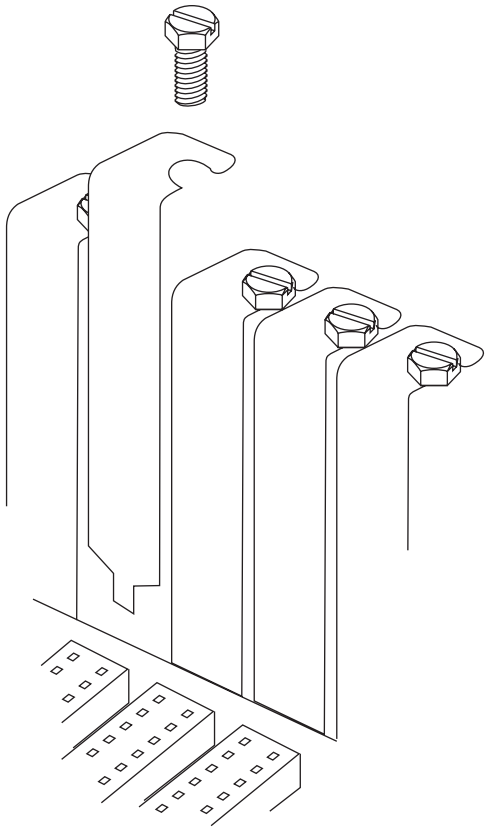


Figure 6. Computer expansion slots for installing an ISA Buffer card

Figure 7. Removing the expansion slot cover on an AT type computer



- Remove the expansion slot cover on the rear panel of the I/O slot selected (see Figure 7).
- Insert the ISA Serial Buffer Board as far as possible into the appropriate socket, ISA or EISA. Then secure the Serial Buffer Board by reinstalling the expansion slot cover screw.
- Connect the serial cable to the nine-pin cable on the Serial Buffer Board mounting panel. The other end of the serial cable connects to the Controller's Serial Output connector (item 20 of Figure 2). Take care to tighten the screws at both ends of the cable using a small, flat-bladed screwdriver.

Checking the ISA Serial Buffer Board

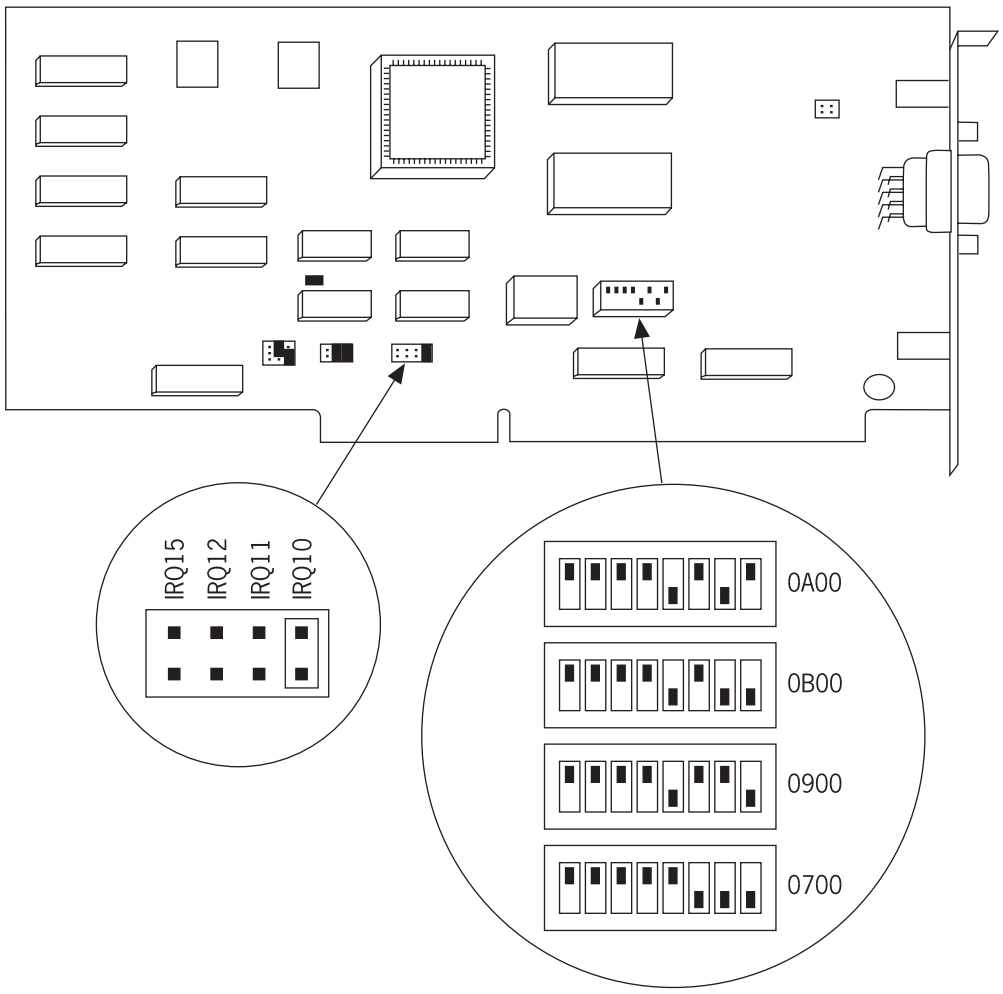
Now that the ISA board is installed, its address should be confirmed. The factory default address is 0A00. This address can be confirmed or changed by comparing the 8 dip switches found on the board with Figure 8. The ISA Serial Buffer board is set to interrupt level 10 and uses DMA channels 5 and 6. The interrupt level can be changed by the user, as long as both hardware and software are set to the same interrupt. Figure 8 shows all possible configurations. If the default DMA channels present a problem, contact the factory for more information.

CAUTION

Since interrupts and DMA channels cannot be shared, make sure no other boards in your computer use this interrupt or these DMA channels.

Replace the cover of the computer and turn on the computer only. If an error occurs at boot up, either the Serial Buffer Board is not installed properly or the address is set incorrectly. Turn off the computer, verify the address setting and check that the Serial Buffer Board is firmly mounted in the slot.

Figure 8. ISA board switch and jumper settings



NuBus Serial Buffer Board

Introduction

If the computer is an Apple Macintosh II, a NuBus Serial Buffer board must be installed as follows.

Installation Steps

A screwdriver may be needed to remove screws from the computer (the type varies from computer to computer). A small, flat-bladed screwdriver will additionally be needed to tighten the screws that secure both ends of the serial cable.

- Make sure the computer power switch is turned off. Then remove the computer chassis cover. The appropriate slots for installing a NuBus card are shown in Figure 9 above.
- Remove the expansion slot cover on the rear panel of the I/O slot selected (see Figure 10).

Figure 9. Computer expansion slots for installing NuBus serial card

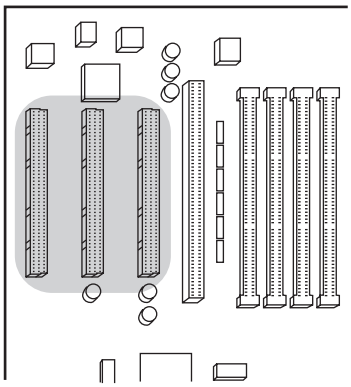
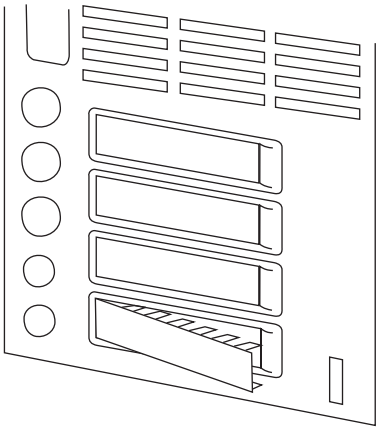


Figure 10. Removing the expansion slot cover on a Macintosh computer



- Insert the Serial Buffer Board into the computer chassis and insert it as far as possible into the appropriate NuBus socket. Then secure the Serial Buffer Board by reinstalling the expansion slot cover screw.
- Connect the serial cable to the nine-pin cable on the Serial Buffer Board mounting panel. The other end of the serial cable connects to the Controller's Serial Output connector (item 20 in Figure 2). Take care to tighten the screws at both ends of the cable using a small, flat-bladed screwdriver.

Checking the NuBus Serial Buffer Board

The NuBus card has no user-changeable jumpers or switches.

Next confirm proper installation of the board by loading and running the application software and then verifying that the expected behavior occurs as described in the software documentation. For example, in the case of IPLab software and the PI

Extension, at boot up, the PI icon will blink once for each NuBus card installed. If proper startup doesn't occur, turn off the computer and make sure the card is correctly installed.

Parallel Buffer Board

Installation

- Make sure the power switch is turned off. Remove the computer chassis cover.
- Remove the expansion slot cover on the rear panel of the I/O slot selected. This procedure for AT type computers is shown in Figure 4 on the left.
- On the Parallel Buffer Board locate the strain relief, an aluminum bracket on the edge of the board. This is labeled "1" in Figure 11. Remove the bottom screw (Phillips) that holds the cable strain relief (number 3 on the same figure) and put the screw aside. Do not remove the top screw (Allen type), and do not insert the board completely into the slot yet.
- Insert the unlabeled ends of the two ribbon cables into the computer through the rear panel as shown in Figure 11. The cable with the gray connector is on the left in Figure 5, furthest from the board. The red stripe of both cables should be on top. Do not damage or remove the copper tape, as it is essential for good grounding.
- Insert the Parallel Buffer Board partway into the computer chassis while opening the strain relief connector (Figure 11, number 1) to accept both ribbon cables.
- Connect the cables, black cable first, as shown in Figure 12. The latches on the card *must* fully close to ensure a viable connection. In Figure 12, part 2 the latches are not yet "locked." Locking is accompanied by a snapping sound. Try to pull the connector loose. This connection is *essential* for proper operation of the system.
- Close the strain relief bracket over the cables and secure it with the Phillips head screw removed earlier (Figure 11, part 3). Being careful not to drop the screw into the computer, install the expansion slot cover screw (Figure 11, part 2).

Once installation is complete the address should be confirmed. See the section below pertaining to the Parallel Buffer Board.

Figure 11. Installing the parallel board

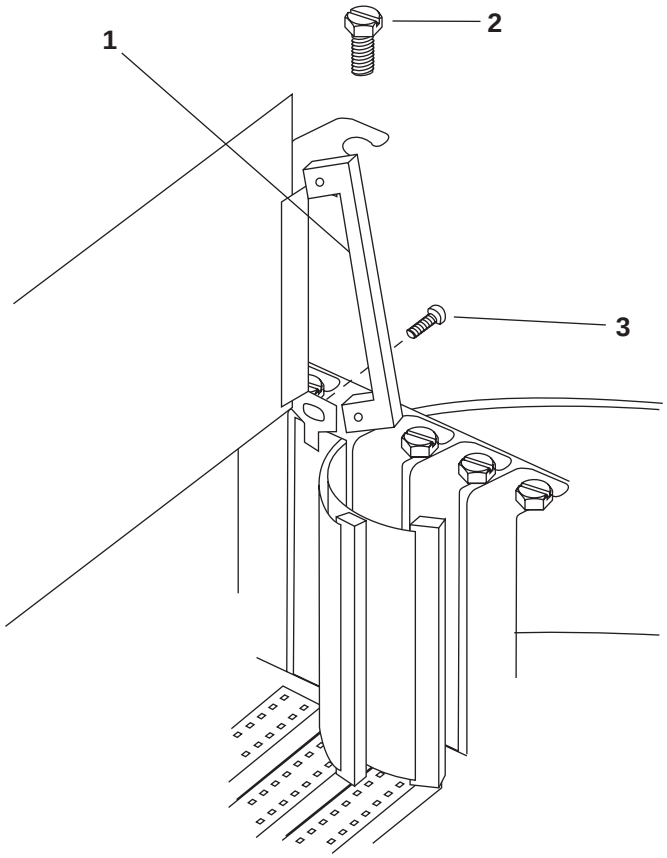
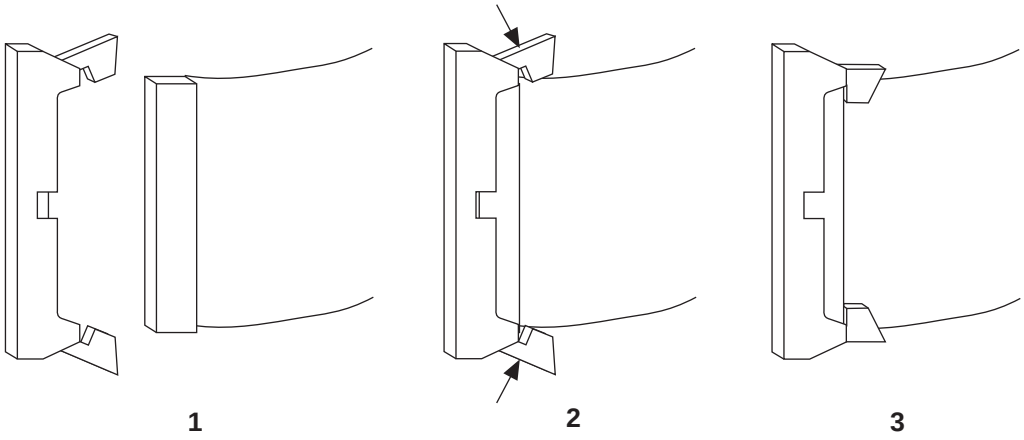


Figure 12. Attaching the parallel interface cables



Checking the Parallel Buffer Board

Now that the Parallel Buffer Board is installed, the address should be confirmed. The factory default address is 09D0. This address can be confirmed or changed by comparing the 16 dip switches found on the board with Figure 13.

CAUTION

Since interrupts and DMA channels cannot be shared by a computer with an ISA bus, make sure no other boards in your computer use this interrupt or these DMA channels.

The Parallel Buffer Board is set to interrupt level 10, and uses DMA channels 5 and 6. The interrupt level can be changed by the user, as long as both hardware and software are set to the same interrupt. Figure 13 shows all possible configurations. If the default DMA channels present a problem, contact the factory for more information.

- Replace the cover of the computer and turn on the computer only. If an error occurs during boot up either the board is not installed properly or the address is set incorrectly. Turn off the computer and check that the board is firmly mounted in the slot.

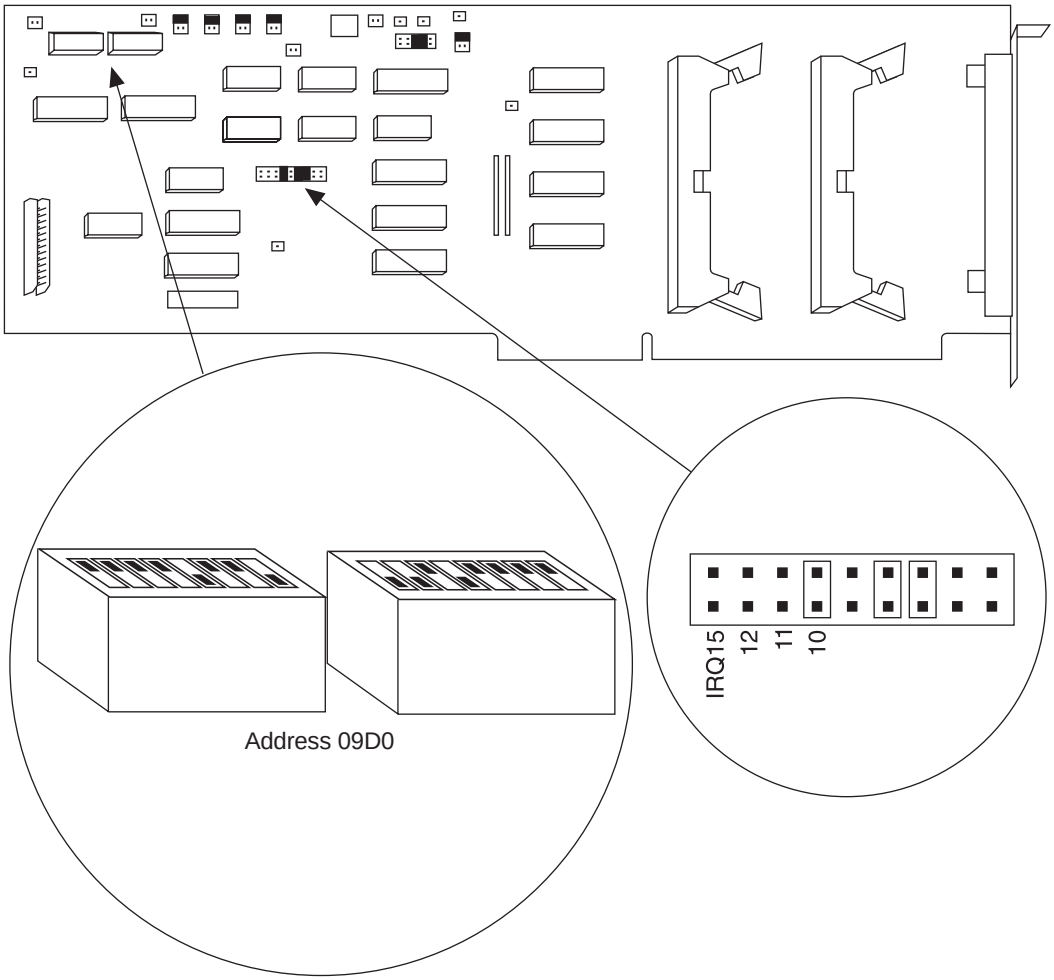


Figure 13. Parallel Buffer Board jumper settings

EISA Serial Buffer Board

Introduction

An EISA Serial board must be plugged into an EISA computer slot or an EISA slot and the Interface type selected from WinView must be "EISA" (not supported in WinView/32).

Installation Steps

CAUTION

For computers with an EISA Interface, special configuration software must be run, sometimes before the card is installed. Read the documentation that came with your computer before attempting to install the EISA serial buffer board.

A screwdriver may be needed to remove screws from the computer (the type varies from computer to computer). A small, flat-bladed screwdriver will additionally be needed to tighten the screws that secure both ends of the serial cable.

Note: EISA and ISA bus connectors are superficially similar, making it possible to mistake an ISA bus computer for an EISA bus computer. Two ways of telling whether the bus is EISA or ISA are by the bus connectors' color and by the number of contacts.

- EISA bus connectors are ***brown***. ISA bus connectors are ***black***.
- ISA bus connectors have either 31 or 49 contacts. The contacts in an EISA bus connector are arranged in two levels, upper and lower. On the upper level are the same 49 contacts as are present on a full-length ISA bus card. On the lower level is a second set of 45 contacts which are only present on EISA bus connectors. However, the location of the lower contacts makes them difficult to see.

- Remove the expansion slot cover on the rear panel of the I/O slot selected.
- Insert the EISA Serial Buffer Board as far as possible into an EISA socket. Then secure the Serial Buffer Board by reinstalling the expansion slot cover screw.
- Connect the serial cable to the nine-pin cable on the Serial Buffer Board mounting panel. The other end of the serial cable connects to the Controller's Serial Output connector (item 20 of Figure 2). Take care to tighten the screws at both ends of the cable using a small, flat-bladed screwdriver.

Checking the EISA Serial Buffer Board

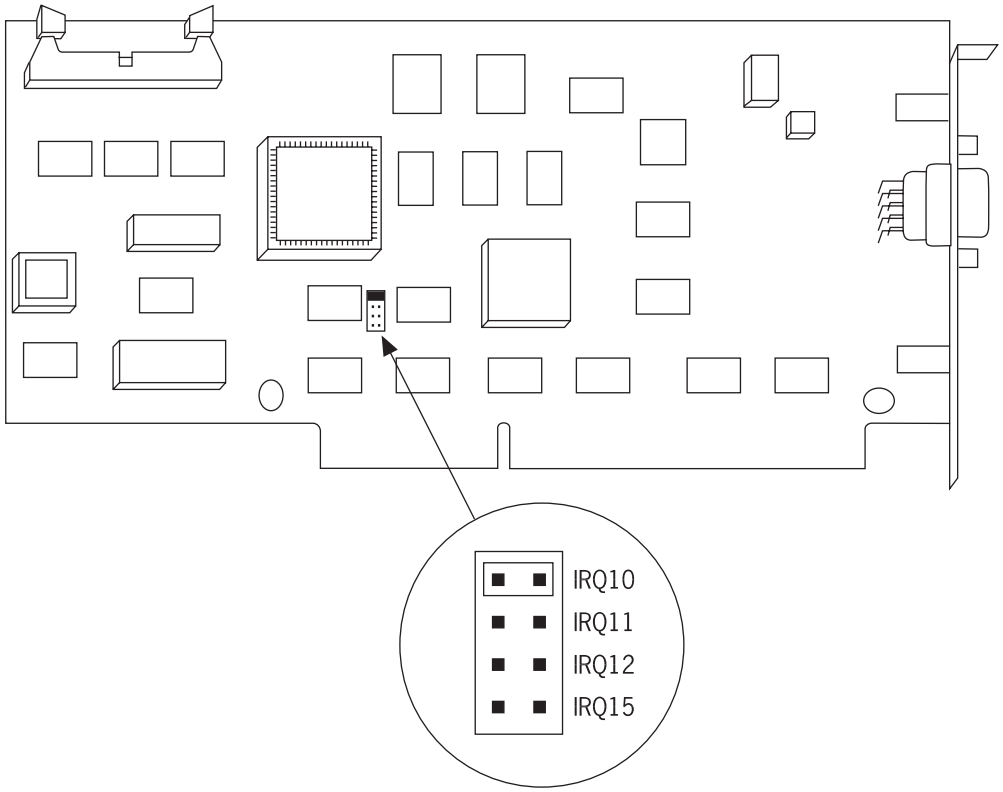
The EISA card address is determined entirely by the where the card is located, slot 1 has address 1000, slot 2 address 2000, and so on. There are no jumpers or dip switches for the user to set the address of an EISA card.

The EISA card is factory set to interrupt level 10. This can be changed by the user, as long as both hardware and software are set to the same interrupt. Figure 14 shows all possible configurations.

- Replace the cover of the computer and continue to configure the computer bus. If an error occurs at boot up, either the Serial Buffer Board is not installed properly or the bus is not properly configured using the configuration software provided by the

computer manufacturer. Turn off the computer and check that the Serial Buffer Board is firmly mounted in the slot.

Figure 14. EISA board jumper settings



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Chapter 4
First Light

Introduction

This chapter provides a step-by-step procedure for placing the system in operation the first time. At this point a lens should be mounted on the camera or the camera mounted on a microscope. *See your camera manual for mounting instructions.* A suggested procedure for operating the system and viewing your first images follows. Note that the intent of this simple procedure is to help you gain basic familiarity with the operation of a ST-130 based system and to demonstrate that it is functioning properly. *An ST-135 based system would be essentially the same but with the difference that communications between the Controller and the Computer would be via an IEEE-488 GPIB Interface. Instructions for configuring GPIB communications are provided in* Once basic familiarity has been established, then operation with other operating configurations, ones with more complex timing modes, can be established as described in Chapter 6, *Experiment Timing*.

To carry out this procedure, it will be necessary to have a basic grasp of the applications software. Refer to your software manual for the required information.

WARNING

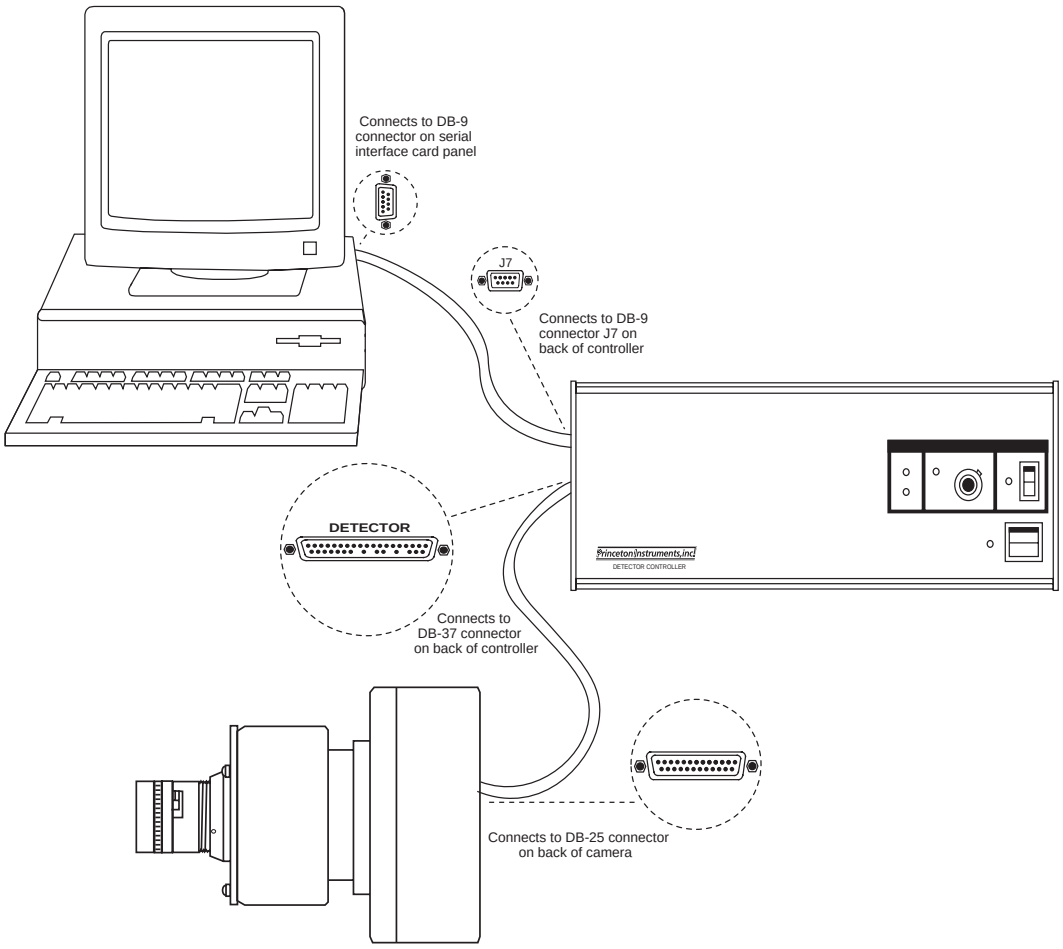
Before You Start, if your system includes a microscope Xenon or Hg arc lamp, it is **CRITICAL** to turn off all electronics adjacent to the arc lamp, especially your digital camera system and your computer hardware (monitors included) before turning on the lamp power.

Powering up a microscope Xenon or Hg arc lamp causes a large EMF spike to be produced that can cause damage to electronics that are running in the vicinity of the lamp. We advise that you place a clear warning sign on the power button of your arc lamp reminding all workers to follow this procedure. While RS Princeton Instruments has taken great care to isolate its sensitive circuitry from EMF sources, we cannot guarantee that this protection will be sufficient for all EMF bursts. *Therefore, in order to fully guarantee the performance of your system, you must follow this startup procedure.*

Procedure

- If the system cables haven't as yet been installed, connect them as follows (system power off). *See Figure 15.*
  - Connect the 25 pin cable from the **DETECTOR** connector on the back of the ST-138 to the mating connector at the camera. Be sure to secure the cable at both ends.

Figure 15. System connection diagram



- Connect one end of the 9 pin serial cable to J7 on the back of the ST-138. Connect the other end of the cable to the DB-9 connector on the panel of the serial interface card.
- Connect the line cord from the Power Input assembly on the back of the controller to a suitable source of AC power.

- If you haven't already done so, install a lens on the camera or connect it to your microscope or other system optics, whichever applies. *See the manual for your particular camera.* The initial lens settings aren't important but it may prove convenient to set the focus to approximately the anticipated distance and to begin with a small aperture setting.
- After reviewing the operating directions for your particular software and camera, follow the directions in those manuals and begin data acquisition. Take care to observe all equipment and personnel safety requirements as outlined in your camera manual.
- Adjust the lens aperture, intensity scaling, and focus for the best image. Some imaging tips follow.
- Begin with the lens blocked off. Set the lens at the smallest possible aperture (largest f-stop number).

WARNING

If using an intensified camera, it is critical to follow the procedures in the camera manual precisely, and to comply with the requirements of all the manual cautions and warnings. When powered, an intensified camera can be destroyed in a few seconds by light overload.

- Place a suitable target in front of the lens. An object with text or graphics works best. If working with a microscope, use any easily viewed specimen. It is generally not advisable to attempt fluorescence imaging during this *Getting Started* phase of operation.
- Set the focus adjustment of the lens for maximum sharpness in the viewed image.
- In the case of a camera with an F-mount, the camera lens adapter itself also has a focus adjustment. If necessary, this focus can be changed to bring the image into range of the lens focus adjustment. See your camera manual for instructions on how to do this.
- Once optimum focus and aperture have been achieved, you can switch from focusing to standard data-acquisition operation. *In WinView you might want to begin with Free Run Asynchronous operation while gaining basic system familiarity*.

This completes *First Light*. If the system functioned as described, you can be reasonably sure it has arrived in good working order. In addition, you should have a basic understanding of how the system hardware is used.

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Chapter 5

Temperature Control

Temperature control is done via Temperature knob on the front panel of the ST-130. *Figure 16 shows the dial settings for two different temperatures.* Once the cooler power is turned on and the desired array temperature has been set, the ST-130 controls the thermoelectric cooling circuits in the camera so as to reduce the array temperature to the set value. On reaching that temperature, the control loop locks to the set temperature for stable and reproducible performance. The green Temperature Status indicator on the front panel lights to indicate that temperature lock has been reached (temperature within 0.05°C of set value). If using WinView, there will also be a **Temperature Locked YES** indication in the Detector Temperature dialog box (accessed from the Setup menu). This on-screen indication allows easy verification of temperature lock in experiments where the computer and controller are widely separated. There is also provision for reading out the actual temperature at the computer so that the progress of the cooldown can be monitored.

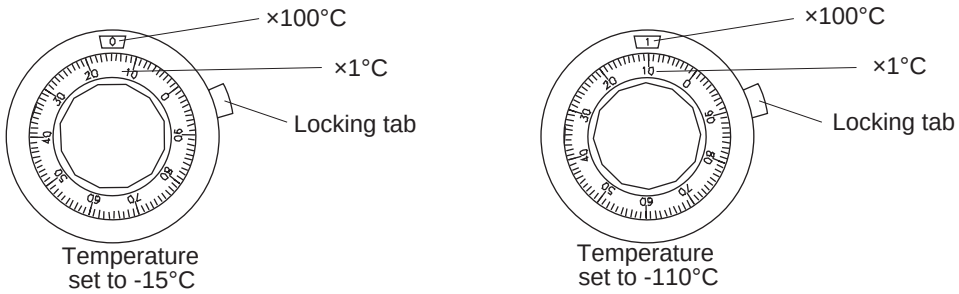


Figure 16. Temperature dial set to -15℃ and to -110℃

There is additionally a red warning temperature indicator. Specifically, it lights if the temperature is set below -75°C with a type TE detector or below -140°C with a type LN detector. Clearly, if the red indicator is lighted, it will be impossible to achieve temperature lock. *However, depending on the camera model, array type and other factors, it will probably not be possible to achieve lock at temperatures well above those required to light the red indicator.*

As protection against damage from overheating, PI cameras are equipped with a thermal-protection switch that interrupts power to the cooler circuits if the internal temperature exceeds +50°C. This protection is effective for temperature settings down to approximately -270°C

WARNING

Do not operate with temperature settings outside the range of your particular camera! At temperature settings below approximately -270°C, an overheating condition will occur that could cause internal damage to the camera after an extended period of operation.

Because the control loop is designed to achieve temperature lock as quickly as possible, overshoot may occur. If this happens, the green Temperature Status indicator will light, then extinguish briefly during the overshoot, then light again and remain lighted as stable control is re-established. This is normal behavior and should not be a cause for concern. Should a low temperature be set initially and then a higher one, this overshoot would probably not occur because the temperature control loop doesn't drive the temperature higher, but rather waits passively for temperature rise to occur. Optimum noise performance is achieved by operating at the lowest temperature at which temperature lock can be maintained. Typical values for the lowest temperature can vary over a wide range and will depend on a number of factors, including the camera and array type, as discussed in the individual camera manuals.

Temperature lock to a temperature in the normal operating range for a type TE or RTE camera should typically take about ten minutes. However, the time required to achieve lock can vary over a considerable range, depending on such factors as the camera type, CCD array type, type of cooling, etc. Also, if the lab is particularly warm, achieving temperature lock might take a little longer (30 minutes maximum), or the lowest temperature at which lock can be achieved could be a little higher. Once lock occurs, it's okay to begin focusing. However, you should wait an additional twenty minutes before taking quantitative data so that the system has time to achieve optimum thermal stability.

Jumper Settings

Users who have purchased only one detector and one shutter should never need to change the jumpers and switches within the controller. Your equipment is tested as a complete system at the factory, and all of these settings have been verified.

If you plan to use more than one detector or more than one shutter with this controller, the jumpers and switches may need to be changed for each detector. See Appendix B for the appropriate settings.

Detector Setup

Since each type of detector has its own specifications and warnings, the setup instructions for your detector are contained in a separate manual. The remainder of this manual is devoted to describing the timing and readout features of this RS Princeton Instruments system.

Chapter 6
Experiment Timing

The RS Princeton Instruments system has been designed to allow the greatest possible flexibility when synchronizing data collection with an experiment. Below are listed the different timing configurations.

TE/CCD, LN/CCD, and ICCD users can apply any of the timing modes below to their experimental setup. ICCD users also have the option of using a HV pulser, which offers additional gating modes. These gating modes are described in the pulser manual.

The chart below lists all of the timing mode combinations. Use this chart in combination with the detailed descriptions in this chapter to determine the optimal timing configuration.

Table 2. Detector timing modes.

Mode	Store Enable	Shutter
Freerun	Off	Normal
Freerun	On	Normal
External Sync	Off	Normal
External Sync	Off	Preopen
External Sync	On	Normal
External Sync	On	Preopen

Synchronous or Asynchronous

The parameter determining overall control of the experiment timing is called Synchronous by the software. When Synchronous is not selected, the controller is operating in Asynchronous mode.

Note: In the case of WinView/32 and WinSpec/32, the term **Full Speed** is also used to designate Synchronous operation and **Safe Mode** is used to designate Asynchronous operation.

Figure 17 is a flow chart comparing the Synchronous and Asynchronous modes. In Synchronous mode, the controller runs according to the timing of the experiment, with no interruptions from the computer. In Asynchronous mode the computer processes each frame as it is received. The controller cannot collect a frame until the previous frame has been completely processed.

Synchronous mode is primarily for collection of “real” experimental data, where timing is critical and events cannot be missed. Once the controller is sent the STARTACQ

command from the computer, all frames are collected by the controller without further intervention from the computer. A Trigger Out pulse from the controller indicates the beginning of the first exposure (the controller sends only one Trigger Out for the entire series of frames). The advantage of this timing mode is that timing is controlled completely through hardware. A drawback to this mode is that the computer will only display frames when it is not performing other tasks. Image display has a lower priority, so the image on the screen may lag several images behind. A second drawback is that a data overrun may occur if the number of images collected exceeds the amount of allocated RAM.

When collecting more than one frame in Synchronous mode the shutter may open one too many times, or perhaps only open partway on this last exposure. This phenomenon occurs when the controller begins an exposure before the computer issues the STOPACQ command, the command that instructs the controller to stop acquiring data. The extra and/or partial exposure is not digitized or stored, so if the controller is programmed to collect 10 frames, the *first* 10 exposures are collected and stored.

Asynchronous mode is primarily useful for experiment setup, including alignment and focusing, when it is necessary to have the most current image displayed on the screen. It is also useful when data collection is part of a macro. As seen in Figure 17, in the Asynchronous mode the computer controls when each frame is taken. A Trigger Out pulse from the controller indicates the beginning of each exposure. After each frame is received the controller sends the STOPACQ command to the controller, instructing it to stop acquisition. Once that frame is completely processed and displayed a STARTACQ is sent from the computer to the controller, allowing it to take the next frame. Display is therefore at most only one frame behind the actual data collection.

One disadvantage of the Asynchronous mode is that events may be missed during the experiment, since after each frame the controller is disabled for a short time. The time delay between each frame acquisition is no longer fixed since the software, which has significantly more jitter than the hardware, has full control of data collection.

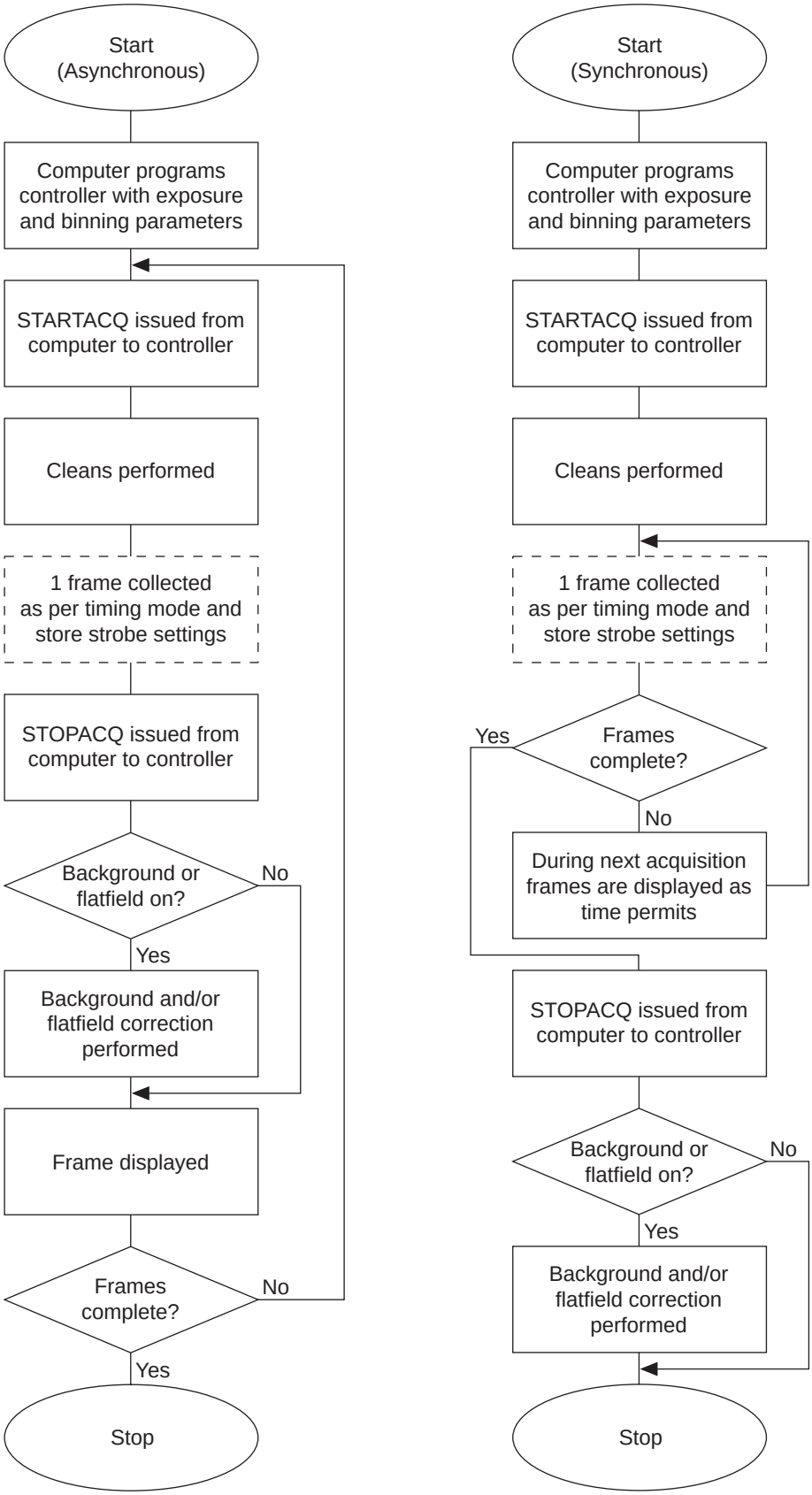


Figure 17. Chart of Synchronous and Asynchronous operation

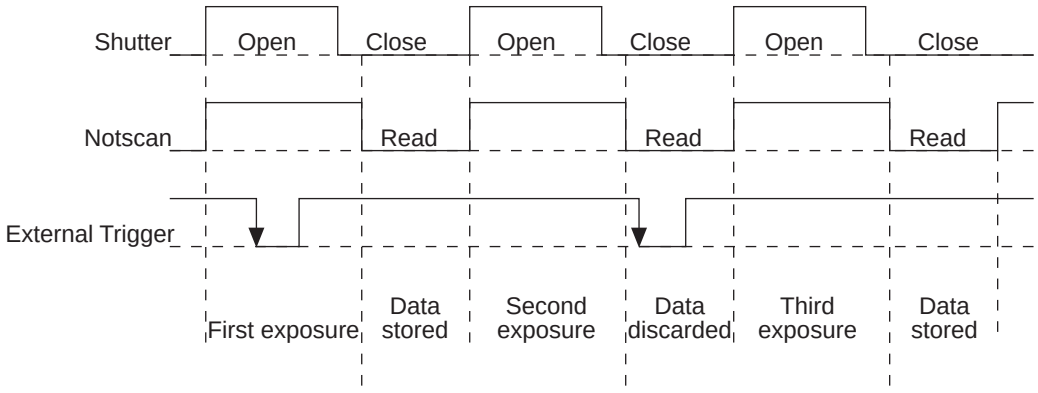
Store Strobe Option

This Store Strobe option is available with all of the standard controller timing modes. It is used when frames must be collected at a constant rate, but only selected ones of these frames need to be stored.

The detector continuously repeats the readout/exposure cycle, either with or without external synchronization. At the start of each readout the controller checks to see if a pulse was received by the External Trigger port on the back of the controller. If an External Trigger was received at any time since the beginning of the previous readout, the digitized data is sent to the computer. If no trigger occurs during this time the digitized data is discarded.

The second trigger pulse in the timing diagram in Figure 18 arrives during a readout. The data that is currently being read out is discarded, but the trigger event is stored in a "latch." At the beginning of the subsequent readout this latch is checked and reset. Since the latch had recorded a pulse, the last readout in the diagram is digitized. In each of the timing mode diagrams, the upper line of text indicates what happens if Store Enable is not selected. The lower line of text, below the External Trigger plot, applies if Store Enable is selected. This is the case for Figure 22 and Figure 24.

Figure 18. Store Strobe timing diagram



Once again, this mode is most useful when exposures must always be taken at precise intervals, but where only some of the frames are useful. For data where events are erratic but a background must be subtracted precisely, this option, in combination with one of the timing modes, below offers the highest performance.

The flow chart in Figure 19 shows details of the frame collection portion of Figure 17. The timing mode part of Figure 19 is detailed later in the flow charts in Figure 21 and Figure 23.

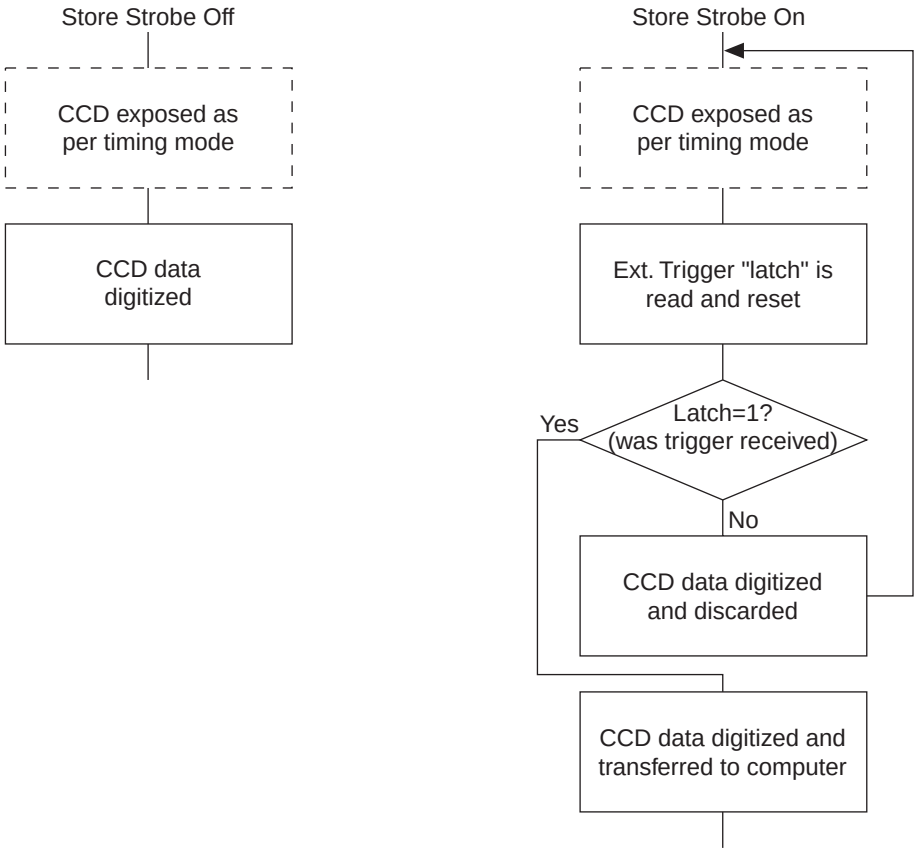


Figure 19. Store Strobe timing chart (ref Figure 17)

Triggering Modes

The triggering modes available for any ST-130 or ST-135 based system are Freerun and External Sync. These timing modes are combined with the Store Enable and Shutter options to provide the widest variety of timing modes for precision experiment synchronization. Cable connections for these timing modes are shown in Figure 20.

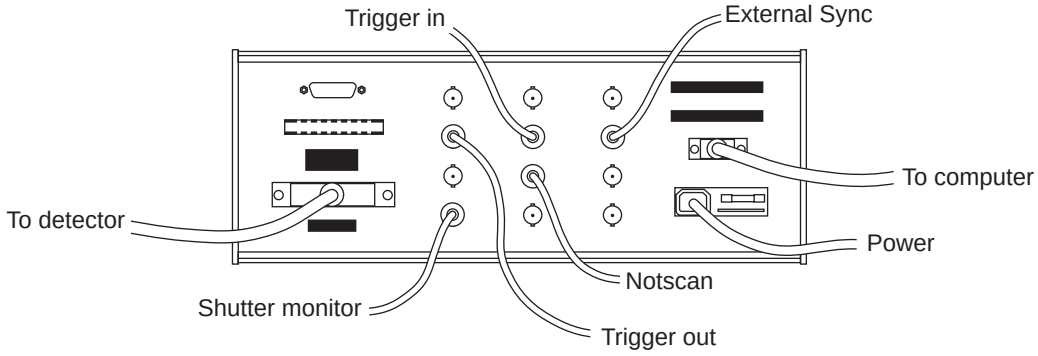


Figure 20. Possible cable connections for timing modes

The shutter options available include Normal, (where no options are selected), Preopen, or Disable. Disable simply means that the shutter will not open at all during the experiment. This is only useful for making dark charge measurements, or when no

shutter is present in the system. Preopen, available in External Sync or Continuous Cleans mode, opens the shutter as soon as the controller is ready to receive an External Sync pulse. This is required if the time between the External Sync pulse and the event is less than a few milliseconds, the time it takes the shutter to open.

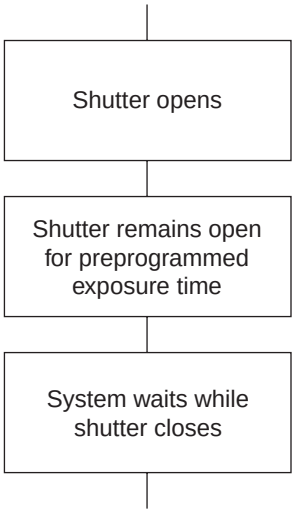
The Shutter Monitor output is shown in the timing diagrams for each timing mode below. Except for Freerun, where the modes of shutter operation are identical, both Normal and Preopen lines are shown in the timing diagrams and flow chart. The flow chart in Figure 19 was represented earlier in Figure 17 as a single box with a dotted line.

The timing diagrams are labeled indicating the exposure time (t_{exp}), shutter compensation time (t_c), and readout time (t_R). These parameters are discussed in more detail in Chapter 7.

Freerun timing

In the Freerun mode the controller does not synchronize with the experiment in any way. The shutter opens as soon as the previous readout is complete, and remains open for the exposure time, t_{exp}. Any External Sync or External Trigger signals are ignored. This mode is useful for experiments with a constant light source, such as a CW laser or a DC lamp. Other experiments that can utilize this mode are high repetition studies, where the number of shots that occur during a single shutter cycle is so large that it appears to be continuous illumination.

Figure 21. Freerun timing chart (ref Figure 19)



Other experimental equipment can be synchronized to the controller by using the Trigger Out, Shutter Monitor, or Notscan ports. These signals (synchronous operation) are shown in Figure 22. All are TTL logic signals, from 0 to 5 V.

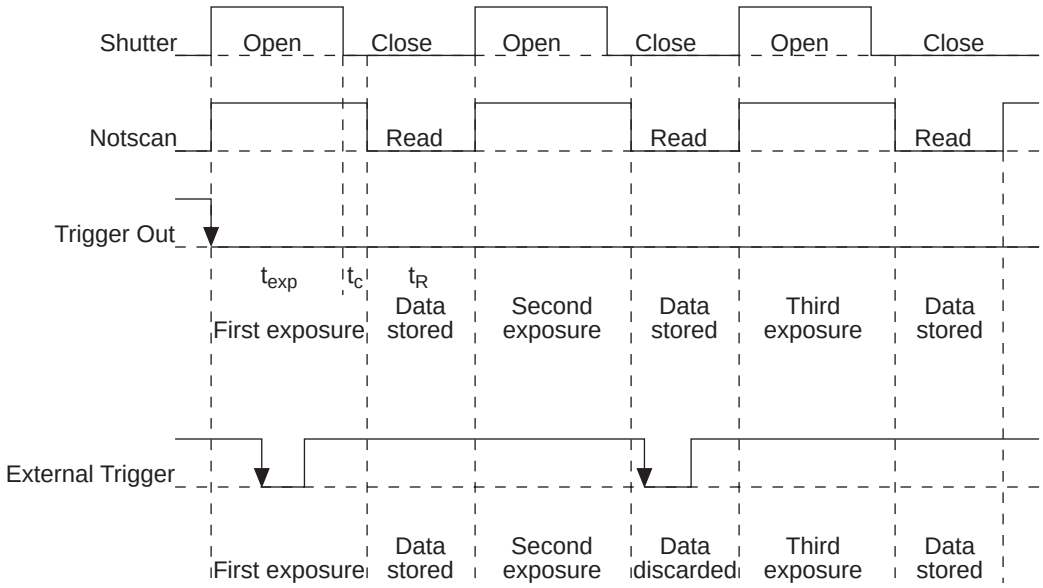


Figure 22. Freerun timing diagram

External Sync timing

In this mode all exposures are synchronized to an external source. As shown in the flow chart, Figure 24, this mode can be used in combination with Normal or Preopen Shutter operation. In Normal Shutter mode, the controller waits for an External Sync pulse, then opens the shutter for the programmed exposure period. As soon as the exposure is complete the shutter closes (shutter compensation time is discussed in Chapter 7) and the CCD data are read out. The shutter requires 5-10 msec to open completely.

Since the shutter requires up to 10 msec to fully open, the External Sync pulse provided by the experiment must precede the actual signal by at least that much time. If not, the shutter will not be open during the entire signal, or the signal may be missed completely.

Also, since the amount of time from the initialization of the experiment to the first trigger pulse is not fixed, an accurate background subtraction may not be possible for the first readout. In multiple-shot experiments this is easily overcome by simply discarding the first frame.

In the Preopen Shutter mode, on the other hand, shutter operation is only partially synchronized to the experiment. As soon as the controller is ready to collect data the shutter opens. Upon arrival of the first External Sync pulse to the controller, the shutter remains open for the specified exposure period, closes, and the CCD is readout. As soon as readout is complete the shutter re-opens and waits for the next frame.

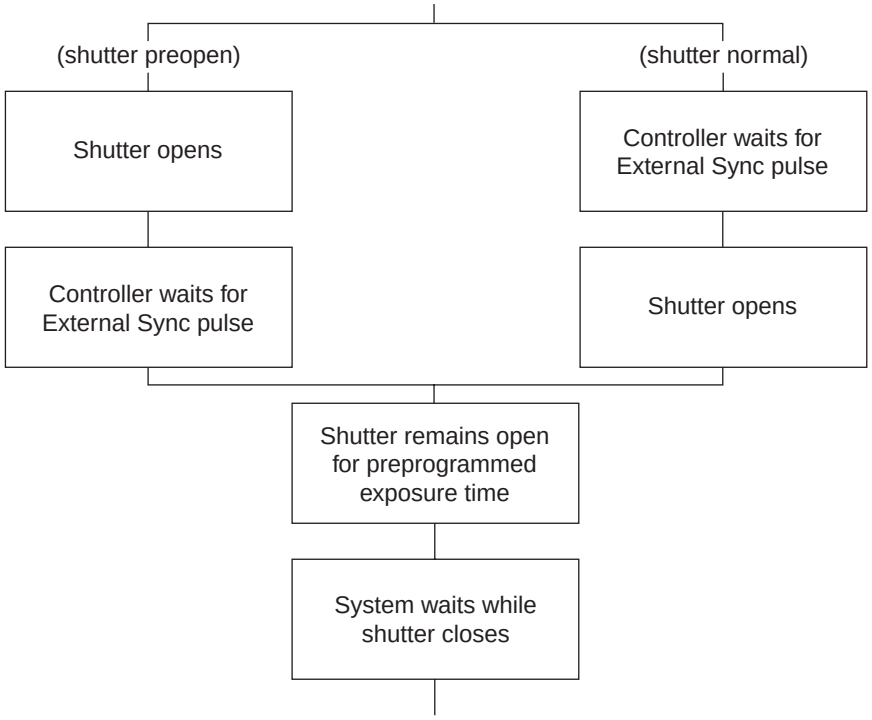


Figure 23. Chart showing two External Sync timing options

The Preopen mode is useful in cases where an External Sync pulse cannot be provided 5-10 msec before the actual signal occurs. Its main drawback is that the CCD is exposed to any ambient light incident on the detector while the shutter is open between frames. If this ambient light is constant, and the triggers occur at regular intervals, this background can also be subtracted, providing that it does not saturate the CCD. As with Normal Shutter mode, accurate background subtraction may not be possible for the first frame.

Also note that in addition to signal from ambient light, dark charge accumulates during the "wait" time (t_w). Any variation in trigger frequency also affects the amount of dark charge, even if light is not falling on the CCD during this time.

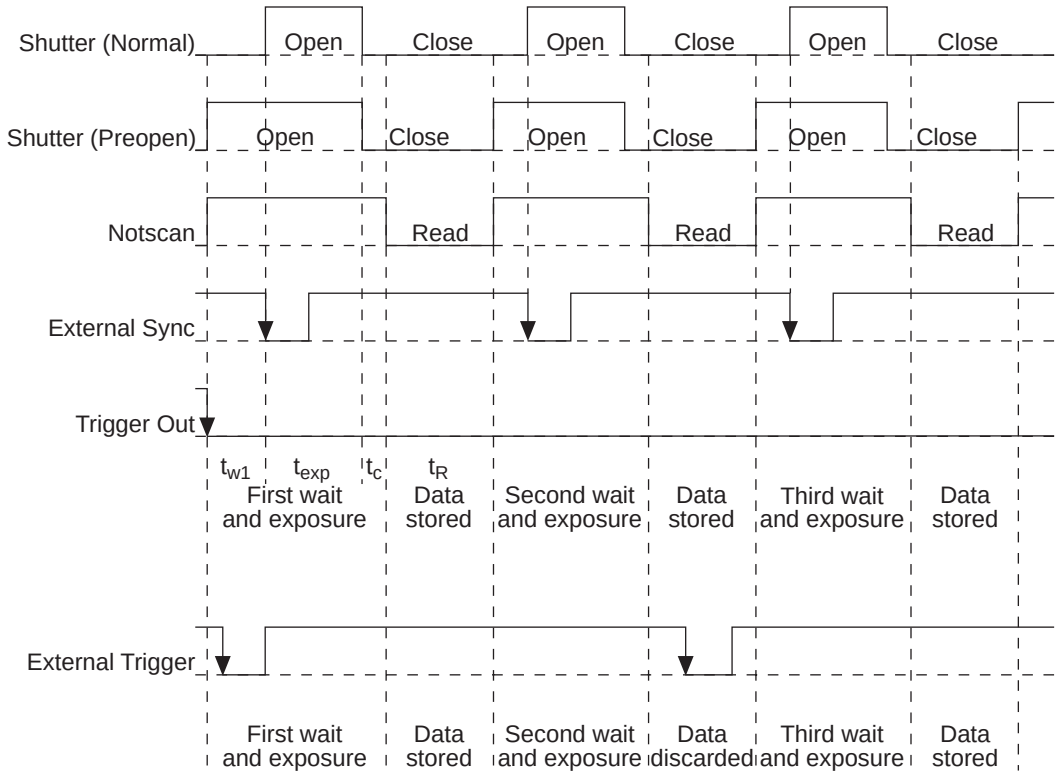


Figure 24. Timing diagram for the External Sync mode

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Chapter 7
Exposure and Readout

Before each image from the CCD detector appears on the computer screen, it must first be read, digitized, and transferred to the computer. A block diagram of the path of the image signal is shown in Figure 25.

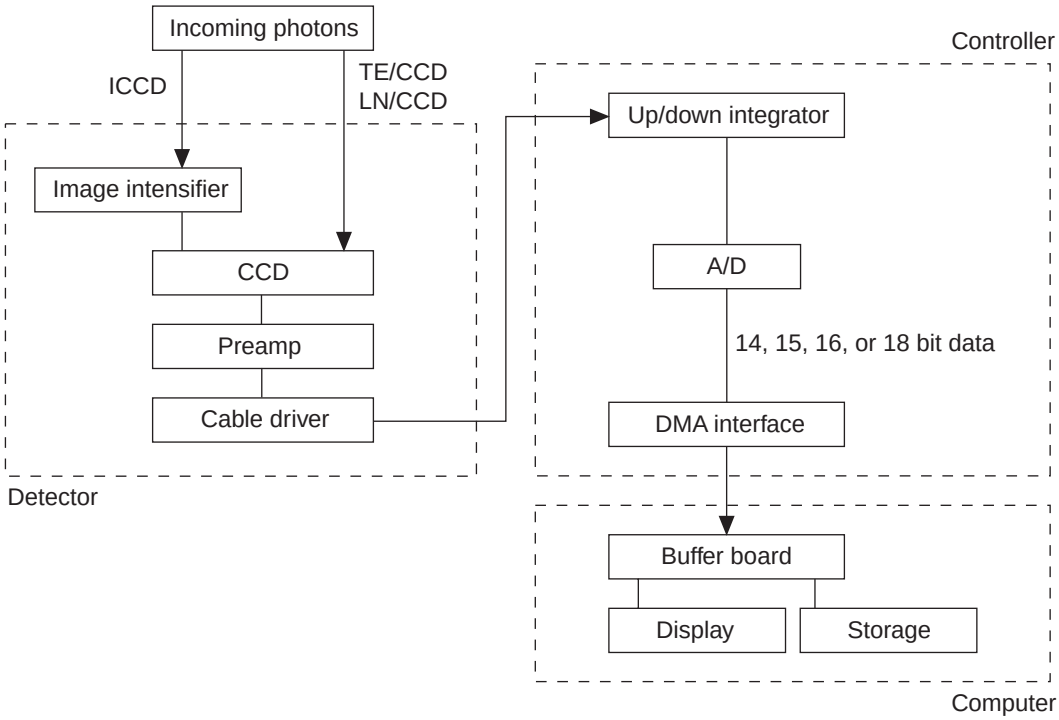


Figure 25. Block diagram of light path in system

The sections below describe the exposure, readout, and digitization of the image, including descriptions of binning for imaging or spectroscopy applications.

Exposure

Charge coupled devices can be roughly thought of as a two dimensional grid of individual photodiodes (called pixels), each connected to its own charge storage “well.” Each pixel senses the intensity of light falling on its collection area, and stores a proportional amount of charge in its associated “well”. Once enough charge accumulates, the pixels are read out serially.

CCD arrays perform three essential functions: photons are transduced to electrons, integrated and stored, and finally read out. CCDs are very compact, rugged, and unintensified, uncoated CCDs can withstand direct exposure to relatively high light

levels and magnetic and RF radiation. They are easily cooled and can be precisely thermostated to within a few tens of millidegrees.

Because CCD detectors, like film and other media, are always sensitive to light, light must not be allowed to fall on the array during readout. Unintensified CCD detectors, including the TE/CCD and LN/CCD models, use a mechanical shutter to prevent light from reaching the CCD during readout. ICCD (intensified) models use an image intensifier to gate the light on and off.

RS Princeton Instruments software allows the user to set the length of time the detector is allowed to integrate the incoming light, called the exposure. During each scan, the shutter or intensifier is enabled for the duration of the exposure period, allowing the pixels to register light.

Exposure with a mechanical shutter

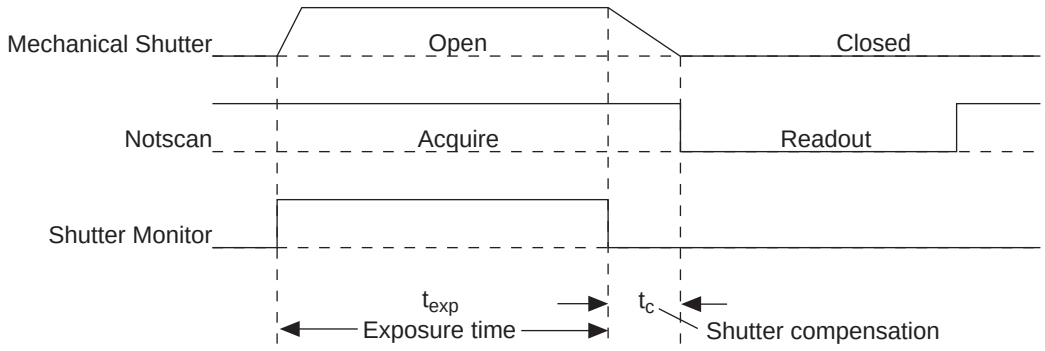
Unintensified CCD detectors, including TE/CCD and LN/CCD models, use a mechanical shutter to control the exposure of the CCD. The following chart lists the appropriate mechanical shutter compensation time (t_c), the delay allowed after the exposure (t_{exp}) for the shutter to close. These values are for detector-mounted shutters only.

Table 3. Shutter compensation time.

CCD Array	Compensation time, msec
576 × 384, 768 × 512, 1317 × 1035	6.75
All other CCDs	26.75

The diagram in Figure 26 shows how the exposure period is measured. Either the Notscan or the Shutter Monitor port on the back of the controller can be used to monitor the exposure and readout cycle (t_R). Both of these signals are also shown in Figure 26.

Figure 26. Exposure of the CCD with shutter compensation



Notscan is low during readout, high during exposure, and high during shutter compensation time. Shutter Monitor is high during exposure, low during shutter compensation, and low during readout.

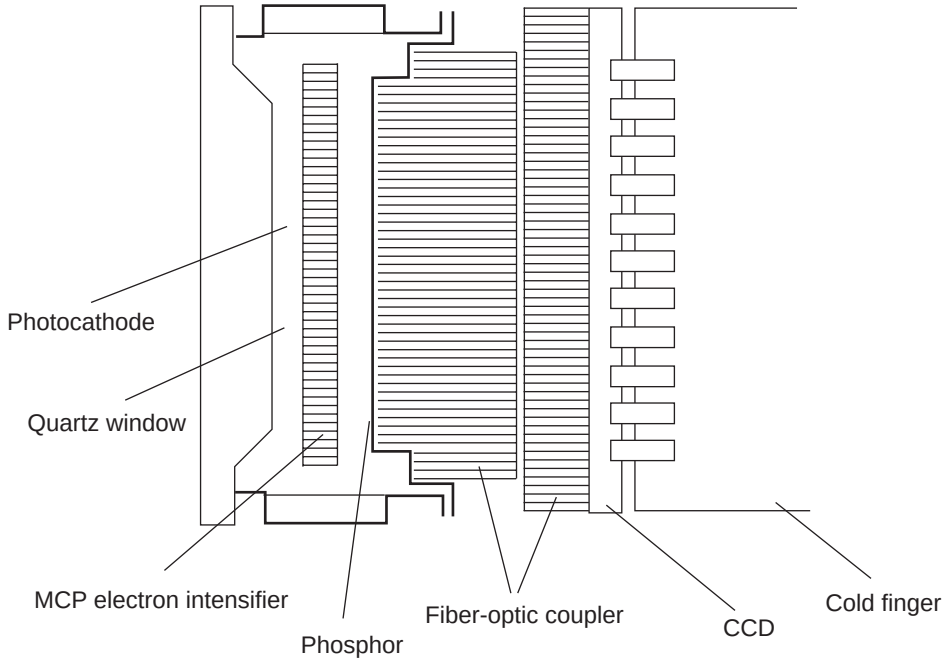
Since most shutters behave like an iris, the opening and closing of the shutter will cause the center of the CCD to be exposed slightly longer than the edges. It is important to realize this physical limitation, particularly when using short exposures.

Exposure with an image intensifier

ICCD (intensified) detectors use an image intensifier both to gate light on and off and to greatly increase the brightness of the image. In these detectors the image intensifier detects and amplifies the light, and the CCD is used for readout. The coupling between the CCD and the intensifier can be either fiber optic, which is the most sensitive, or with a relay lens, a more flexible detector arrangement. With a fiber coupled detector, the combined high gain of the image intensifier and the low readout noise of the CCD array result in a detector capable of responding to a single photoelectron.

The exposure programmed by software in this case refers to duration of gating of the intensifier. Our standard (fiber coupled) ICCD when operated with only a controller is capable of exposures as short as 5 msec. Because the controller is used to control the exposure the shutter compensation time, as shown in Figure 26, is 1.75 msec. For shorter exposures, an RS Princeton Instruments pulser is required.

Figure 27. Diagram of an MCP image intensifier



The MCP (microchannel plate) of the intensifier is composed of more than 10^6 individual miniature electron multipliers with an excellent input to output spatial geometric accuracy. Intensifier gain is varied by adjusting the voltage across the MCP or the voltage across the MCP output and the phosphor. This second parameter is a factory adjustment, as it affects both the gain and the resolution of the intensifier.

Detection of extremely weak CW signals, e.g., luminescence and Raman scattering from solid state samples, is typically limited by the dark current of the intensifier's photocathode, usually referred to as the equivalent brightness intensity (EBI). All standard intensified detectors made by PI have the lowest EBI values possible.

Continuous exposure (no shuttering)

Unlike video rate CCD cameras, slow scan scientific cameras require a shutter to prevent "smearing" of features during readout. This is because during readout, charge is moved horizontally or vertically across the surface of the CCD. If light is falling on the CCD during readout then charge will continue to accumulate, blurring the image along one direction only.

For some experimental applications a shutter is not required because no light falls on the CCD during readout. If the light source can be controlled electronically, outputs such as Trigger Out can produce the signal, and the CCD can be read out in darkness. For some specialized detectors, such as those for some X-ray applications, no shutter is available, and electronic control of the signal is necessary. If a shutter is present it can be held open for short periods of time using the External Shutter Control on the rear of the controller.

In other cases a shutter is not required because "smearing" is not an issue. For spectroscopy applications where only a single spectrum is acquired and the CCD is set up in "parallel" mode (described in the readout section below), smearing of the signal along the slit direction does not cause any loss of information, since no relevant information is contained along the slit axis. By removing or disabling the shutter the highest spectral rates are possible.

Finally, detectors with frame transfer capability may be used with or without a shutter. Although this closely resembles the operation of video rate cameras, the high dynamic range and slower readout may still make the smearing non-negligible. For example, on an 8 bit video rate camera 1% smearing results in only 2 counts of smearing per pixel. On a 16 bit slow scan camera, the same 1% results in over 600 counts of smearing.

Saturation

When signal levels in some part of the image or spectrum are very high, charge generated in one pixel may exceed the "well capacity" of the pixel, spilling over into adjacent pixels in a process called "blooming." In this case a more frequent readout is advisable, with signal averaging to enhance S/N accomplished through the software.

For signal levels low enough to be readout-noise limited, longer exposure times, and therefore longer signal accumulation in the CCD, improves the S/N ratio approximately linearly with the length of exposure time. There is, however, a maximum time limit for on-chip averaging, determined by either the saturation of the CCD by the signal or the loss of dynamic range due to the buildup of dark charge in the pixels (see below).

Dark charge

Dark charge (or dark current) is the thermally induced buildup of charge in the CCD over time. The statistical noise associated with this charge is known as "kT" noise.

Dark charge values vary widely from one detector to another and are exponentially temperature dependent. At -50ºC, a non-MPP CCD will have an average dark charge value of approximately 0.5 counts/pixel/second (approximately 3-6 electrons). This represents approximately 0.003% of a 14-bit A/D (16,000:1). At the typical operating temperature of a TE/CCD or an ICCD, dark charge is reduced by a factor of ~2 for every 7º reduction in temperature. When acquiring data using long exposure times, taking a

dark charge “background image” under identical conditions is essential. This image is subtracted from the raw image in software.

Readout of the Array

In this section, a simple 6 × 4 pixel CCD is used to demonstrate how charge is shifted and digitized. As described below, three different types of readout are available. Full frame readout, for full frame CCDs, reads out the entire CCD surface at the same time. Frame transfer operation assumes half of the CCD is for data collection and half of the array is a temporary storage area. Finally, kinetics operation assumes only a small part of the array is for data collection, and the remainder is for temporarily storing a limited number of frames.

Full frame readout

The upper left drawing in Figure 28 represents a CCD after exposure but before the beginning of readout. The capital letters represent different amounts of charge, including both signal and dark charge. This section explains readout at full resolution, where every pixel is digitized separately.

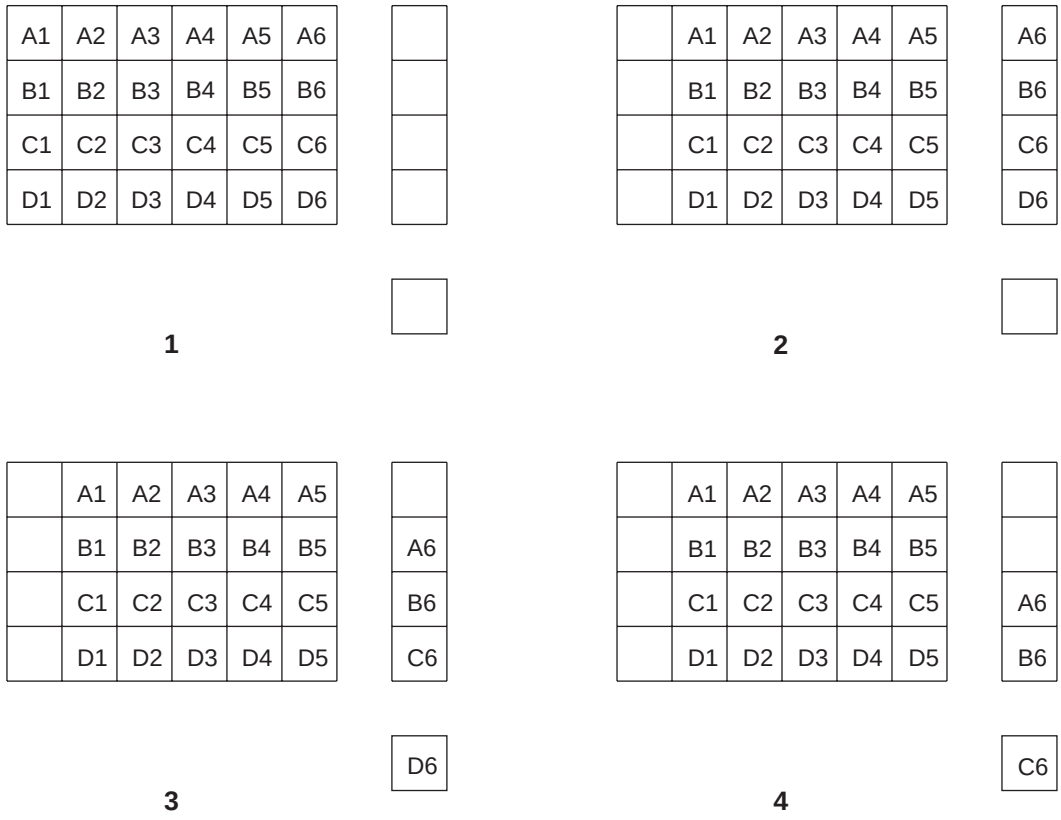


Figure 28. Full frame at full resolution

Readout of the CCD begins with the simultaneous shifting of all pixels one column toward the “shift register,” in this case the column on the far right. The shift register is a single line of pixels along one side of the CCD, not sensitive to light and used for

readout only. Typically the shift register pixels hold twice as much charge as the pixels in the imaging area of the CCD.

After the first column is moved into the shift register, the charge now in the shift register is shifted toward the output node, located at one end of the shift register. As each value is "emptied" into this node it is sent to the controller and digitized. Only after all pixels in the first column are digitized is the second column moved into the shift register. The order of shifting in our example is therefore D6, C6, B6, A6, D5, C5, B5, A5, D4....

After charge is shifted out of each pixel the remaining charge is zero, meaning that the array is immediately ready for the next exposure.

Below are the equations that determine the rate at which the CCD is read out. Tables of values for CCDs supported at the time of the printing of this manual also appear below.

The time needed to take a full frame at full resolution is:

$$t_R + t_{exp} + t_c \tag{1}$$

where

t_R is the CCD readout time,

t_{exp} is the exposure time, and

t_c is the shutter compensation time.

The readout time is given by:

$$t_R = [N_x \cdot N_y \cdot (t_{sr} + t_v)] + (N_x \cdot t_i) \tag{2}$$

where:

N_x is the smaller dimension of the CCD (except for the 1152 × 298, 1152 × 770, and 576 × 384 CCDs, where you should use the larger of the two dimensions)

N_y is the smaller dimension (except in the cases above, where it is the larger)

t_{sr} is the time needed to shift one pixel out of the shift register

t_v is the time needed to digitize a pixel

t_i is the time needed to shift one line into the shift register

(t_s, the time needed to discard a pixel, appears below and in later equations)

Timing values appear below for each CCD array. All clock values are given in microseconds. The numbers below are subject to change, and are therefore not a guarantee that your particular detector will run at a given A/D rate. These values are given as a guideline only.

Table 4. Timing values for each CCD array.

Manufacturer	A/D (kHz)	25	50	100	150	200
SITe TE front illum.	t_i	76.8	38.4	19.2	9.6	9.6
SITe LN front illum.	t_i	76.8	38.4	19.2	9.6	9.6
All SITe back illum	t_i	614.4	307.2	153.6	76.8	76.8
All SITe	t_{sr}	1.2	1.2	1.2	1.2	1.2
All SITe	t_v	43.2	21.6	10.8	5.4	5.4
All SITe	t_s	6.4	3.2	1.6	0.8	0.8
EEV TE cooled	t_i	51.2	25.6	12.8	6.4	6.4
EEV LN cooled	t_i	102.4	51.2	25.6	12.8	12.8
All EEV	t_{sr}	0.6	0.6	0.6	0.6	0.6
All EEV	t_v	40.0	20.0	10.0	6.0	5.0
All EEV	t_s	6.4	3.2	1.6	0.8	0.8
PI front illum.	t_i	76.8	38.4	19.2	N/A	N/A
PI back illum.	t_i	614.4	307.2	153.6	N/A	N/A
All PI	t_{sr}	3.2	3.2	3.2	N/A	N/A
All PI	t_v	43.2	21.6	10.8	N/A	N/A
All PI	t_s	6.4	3.2	1.6	N/A	N/A

A subsection of the CCD can be read out at full resolution, dramatically increasing the readout rate while retaining the highest resolution in the region of interest (ROI). To approximate the readout rate of an ROI, in Equation 2 substitute the x and y dimensions of the ROI in place of the dimensions of the full CCD. A small amount of overhead time is required to read out and discard the unwanted pixels.

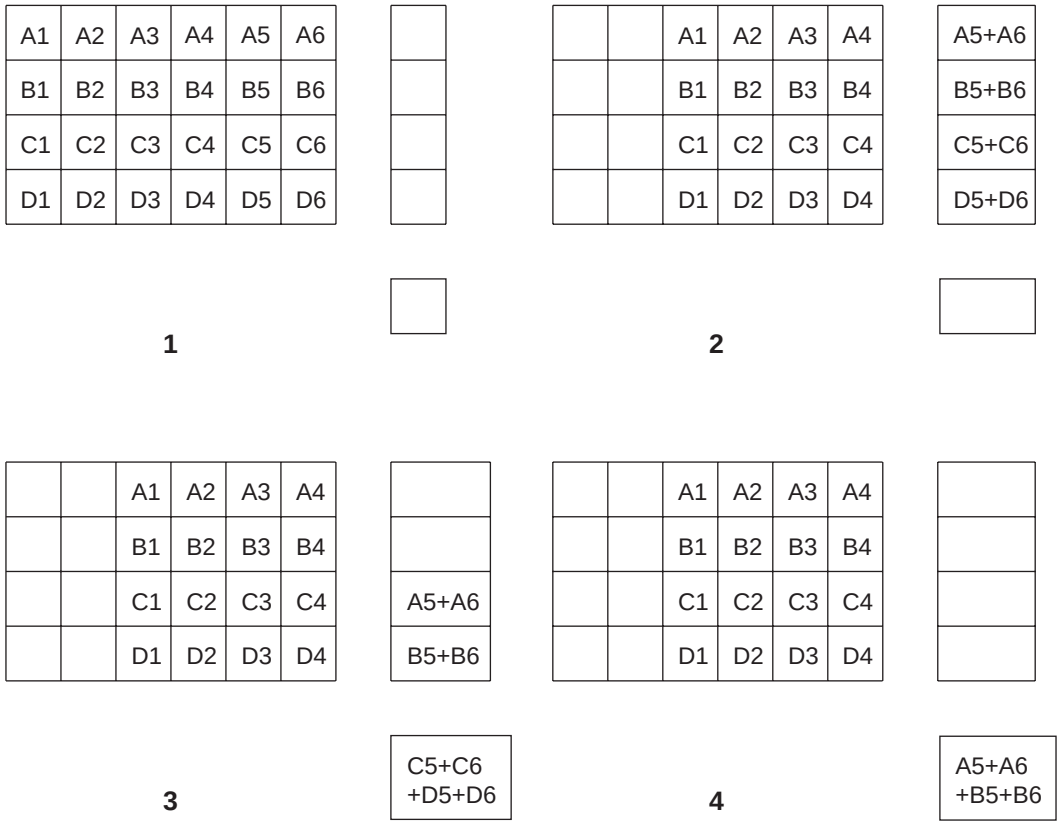
Image readout with binning

Binning is the process of adding the data from adjacent pixels together to form a single pixel (sometimes called a super-pixel), and it can be accomplished in either hardware or software. Rectangular groups of pixels of any size may be binned together, subject to some hardware and software limitations.

Hardware binning is performed *before* the signal is read out by the preamplifier. For signal levels that are readout noise limited this method improves S/N ratio linearly with the number of pixels grouped together. For signals large enough to render the detector photon shot noise limited, and for all fiber-coupled ICCD detectors, the S/N ratio improvement is roughly proportional to the square-root of the number of pixels binned.

Figure 29 shows an example of 2 × 2 binning. Each pixel of the image displayed by the software represents 4 pixels of the CCD array. Rectangular bins of any size are possible.

Figure 29. 2 × 2 binning for images



Binning also reduces readout time and the burden on computer memory, but at the expense of resolution. Since shift register pixels typically hold only twice as much charge as image pixels, the binning of large sections may result in saturation and "blooming", or spilling of charge back into the image area.

The readout rate for n × n binning is calculated using a more general version of the full resolution equation. The modified equation is:

$$t_R = \left[N_x \cdot N_y \cdot \left(\frac{t_{sr}}{n} + \frac{t_v}{n^2} \right) \right] + \left(N_x \cdot t_i \right) \qquad (3)$$

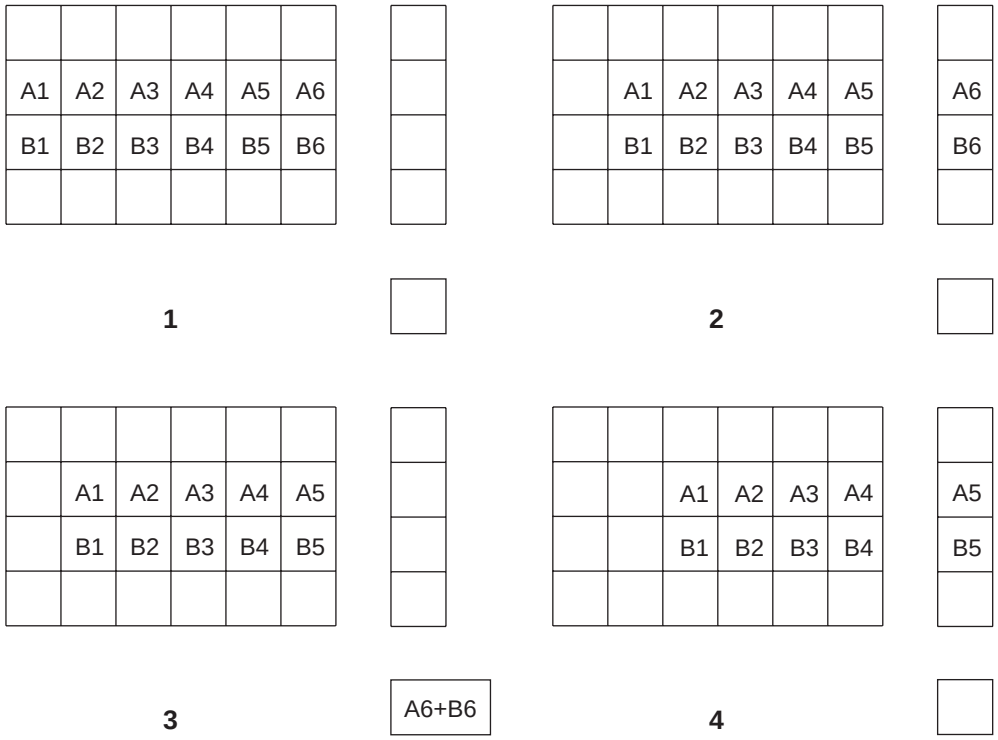
Single spectrum readout with binning

Depending on the physical structure of the CCD, spectroscopic readout is either achieved in “perpendicular” or “parallel” mode. Perpendicular mode is needed when the shift register is along the shorter axis of the CCD, as is the case with 576 × 384, 1152 × 298, and 1152 × 770 formats. All other rectangular formats operate in parallel mode. Square arrays such as the 1024 × 1024 when used for spectroscopic applications can be operated in either perpendicular or parallel mode. See below for a discussion of advantages of both methods.

Perpendicular (slow) mode is best for high light levels, when readout speed is not a factor. Charge cannot “spill” back into the shift register or the image area. Also, the output node can contain ~2-3 times as much charge as an imaging pixel, allowing a larger dynamic range. Finally, readout rate is reduced, since time is required to “empty” the shift register after each vertical shift.

With these arrays each spectral line is first moved to the shift register, then grouped together in the output node and digitized. For the case of our simplified CCD model, shifting proceeds as shown in Figure 30.

Figure 30. Perpendicular mode binning



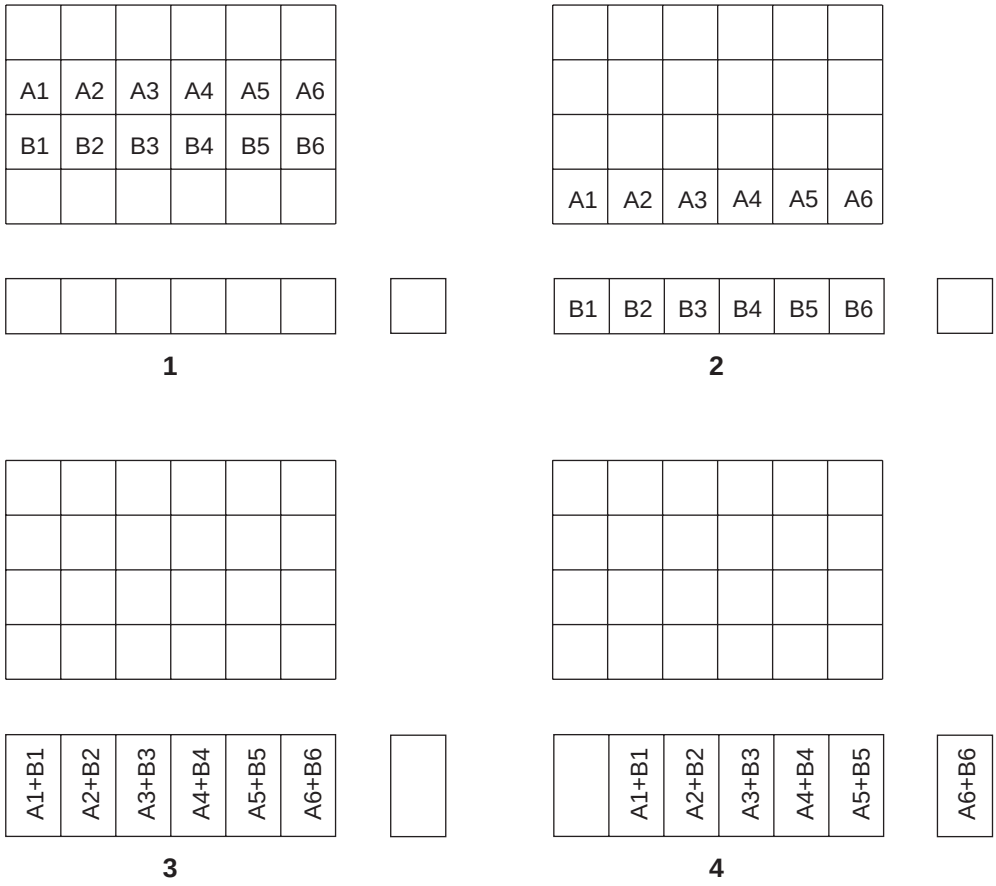
For the perpendicular mode, the equation for binning a single spectrum is:

$$t_R = \left[N_x \cdot N_y \cdot \left(t_{sr} + \frac{t_v}{N_y} + \frac{2t_s}{N_y} \right) \right] + \left(N_x \cdot t_i \right) \quad (4)$$

where t_s is the time needed to discard a pixel (no digitization)

The parallel (fast) mode is used with arrays where the shift register is parallel to the spectral dispersion. Although the dynamic range is now limited by the well capacity of the pixels of the shift register, there is a dramatic increase in speed, since the shift register is only “emptied” once. Figure 31 is a simple example of this mode.

Figure 31. Parallel mode binning



In the parallel mode, the equation for binning a single spectrum becomes

$$t_R = \left[N_x \cdot N_y \cdot \left(\frac{t_{sr}}{N_x} + \frac{t_v}{N_x} \right) \right] + \left(N_x \cdot t_i \right) \qquad (5)$$

Binning in software

One limitation of hardware binning is that the shift register pixels and the output node are typically only 2-3 times the size of imaging pixels. Imaging pixels have a well capacity of approximately 5×10^5 electrons, while shift registers and “binning” capacitors hold approximately 10^6 electrons. Consequently, if the total charge binned together exceeds the capacity of the shift register or output node, the data will be lost.

This restriction strongly limits the number of pixels that may be binned in cases where there is a small signal superimposed on a large background, such as in the case of Raman spectroscopy of signals with a large fluorescence. Ideally, one would like to bin many pixels to increase the S/N ratio of the weak peaks but cannot, since the fluorescence will quickly saturate the CCD.

The solution is to perform the binning in software. Limited hardware binning may be used when reading out the CCD. Additional binning is accomplished in software, producing a result that represents many more photons than was possible using hardware binning.

Software averaging can improve the S/N ratio by as much as the square root of the number of scans. Unfortunately with a high number of scans, i.e., above 100, detector 1/f noise may reduce the actual S/N ratio to slightly below this theoretical value. Also, if the light source used is photon flicker rather than photon shot noise limited, this theoretical signal improvement cannot be fully realized. Again, background subtraction from the raw data is necessary.

This technique is also useful in high light level experiments, where the detector is again photon shot noise limited. Summing multiple pixels in software corresponds to collecting more photons, and results in a better S/N ratio in the measurement.

Digitization

During readout, an analog signal representing the charge of each pixel (or binned group of pixels) is sent to the controller and digitized. The number of bits per pixel is based on both the hardware settings and the settings programmed into the controller through the software.

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Appendix A
Specifications

General

Thermostating Precision:	±0.05°C
A/D Converter Range:	12, 14-18 bits
Linearity:	better than 1%.
Exposure (Integration Time):	5 msec to 23 hours
Readout Rate:	25, 50, 100, 150, 200 kHz, depending on converter
Readout Noise:	1-3 counts RMS on standard systems
Dimensions:	7″ h, 17″ w, 16″ d; rack mounts available
Weight:	18 kg
Power Requirements:	100, 120, 220, or 240 V at 50 or 60 Hz, approximately 250 W. *100 V range is not available with 18 bit A/D.*
TTL Requirements:	Rise time ≤ 40 nsec, Duration ≥ 100 nsec

Input Ports

External Synchronization:	TTL low; up to $1/t_R$
Trigger In:	TTL low
Normalize Input (Source Comp.):	0 to +10 V
External Shutter Control:	TTL low to open shutter, high to close
Software Programmable Inputs:	(8) TTL low or high

Output Ports

Trigger Out:	TTL low at start of data acquisition
Notscan:	TTL high during exposure; low during readout.
Shutter Monitor Out:	TTL high when energized; low when deenergized.
Software Programmable Outputs:	(4) TTL low or high, (4) high voltage (60 V, 0.5 A) for use with relays, etc.

Shutter

CCD Type	Open time	Close time
576 × 384, 768 × 512, 1317 × 1035	5 msec	6 msec
All other CCDs	10 msec	20-25 msec
Entrance slit shutter	5 msec	6 msec
ICCD in CW mode	1.5 msec	1.5 msec

Appendix B
Internal Settings

The ST-130 and ST-135 Controllers use several sets of jumpers to define various parameters. Most of these jumpers have a unique correct orientation, and all have been set at the factory. The user is therefore not encouraged to remove the top cover of the controller unnecessarily. A few settings, however, depend on the user's experimental requirements, and may need to be changed. Each jumper that is settable by the user is shown below and listed on the following page.

CAUTION Unplug line cord before removing top cover.

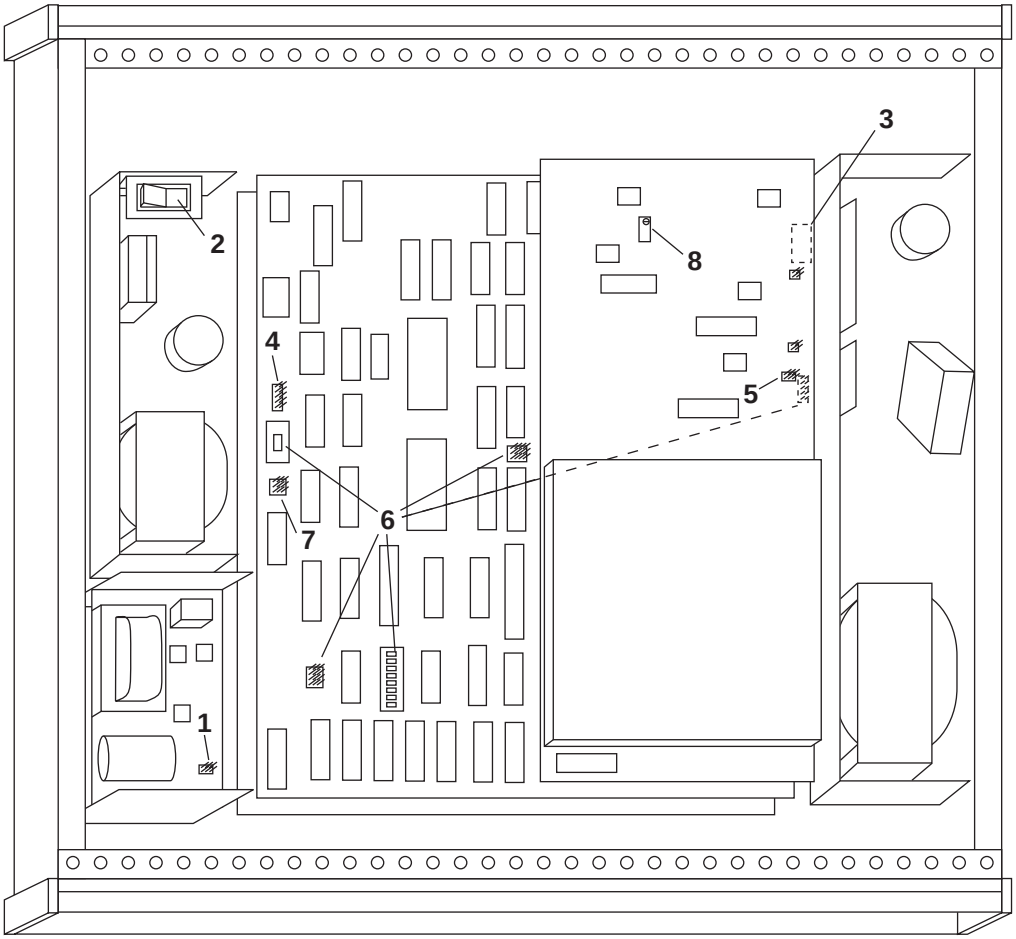
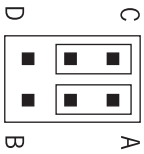
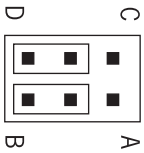


Figure 32. Internal settings of the ST-130 and ST-135 Controllers

	Label	Description
Shutter Selection		
1.	JP1	Set the shutter driver board selector jumper as shown below



1" and 40 mm shutters
(all detector mounted shutters)



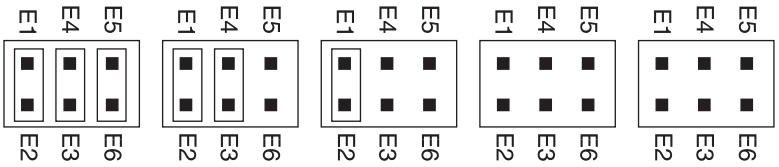
all slit-mounted shutters
(spectroscopic applications only)

LN or TE Selection		
2.		Temperature Control Selection Switch. For LN cooled detectors, switch should be toward the “LN/CCD” label. For TE cooled detectors (including ICCDs), switch towards the “OTHER” label.
3.	SW1	Position switch towards the front panel for LN and towards the rear panel for TE cooled detectors as indicated on the circuit board.

Note: Both switches 2 and 3 must be set to the same detector type.

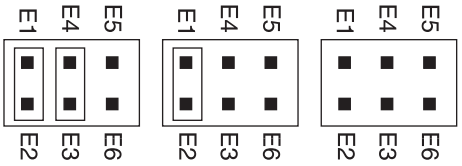
A/D Speed and System Gain		
4.	JP5	Selects the readout rate. Increasing the readout rate above the factory setting may increase the readout noise slightly, causing 16 bit systems to not retain its full 16 bits of resolution.
5.	E Jumpers	The E Jumpers set the gain of the system to match the readout rate. Whenever the readout rate is changed, the E Jumpers must also be reset as shown on the following page.

Jumpers for 14-bit, 15-bit or 16-bit Controller



25 kHz 50 kHz 100 kHz 150 kHz 200 kHz

Jumpers for 18-bit Controller

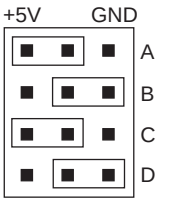
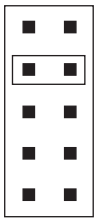
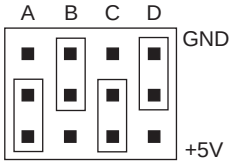
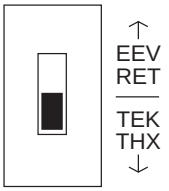
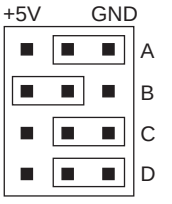
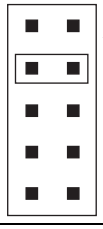
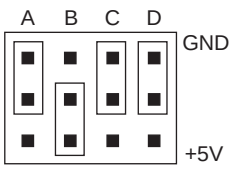
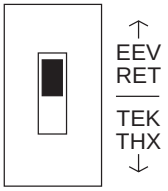
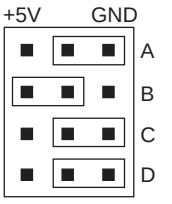
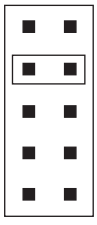
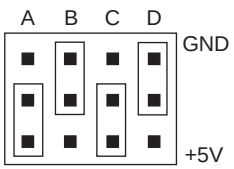
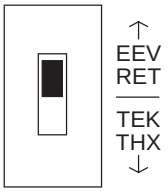


25 kHz 50 kHz 100 kHz

Clock Speed

6. JP6,JP7,JP8,SW2,SW3 Clock speed selection jumpers. These only need to be changed if operating more than one detector. Set according to Table 5 and Table 6.

Table 5. Jumper settings.

	JP6	JP7	JP8	SW2
All SITe (TEK)				
EEV 3 phase (except some 1024×256)				
EEV 6 phase, some 1024×256 & PI 1340 devices				

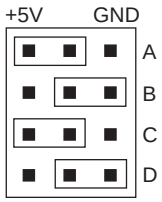
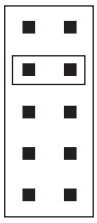
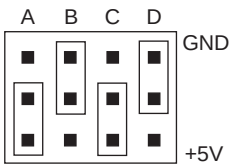
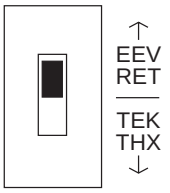
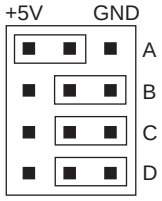
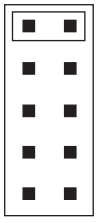
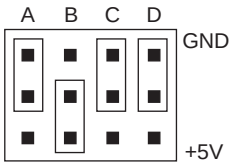
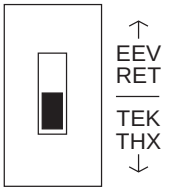
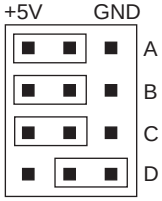
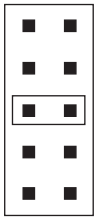
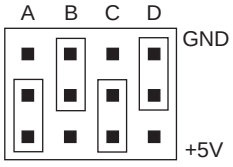
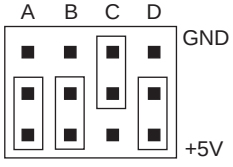
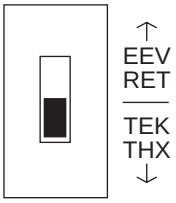
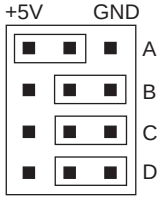
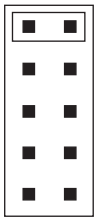
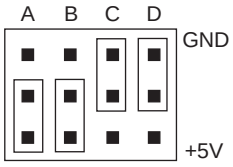
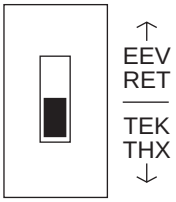
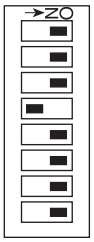
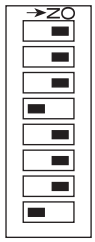
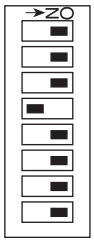
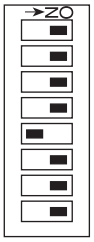
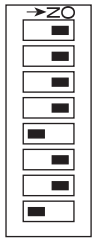
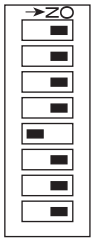
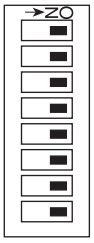
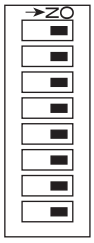
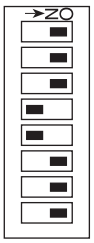
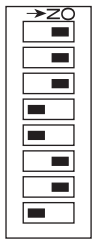
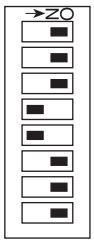
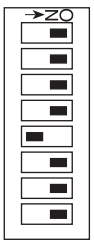
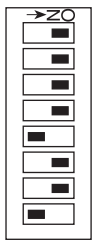
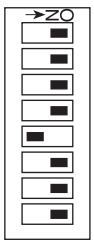
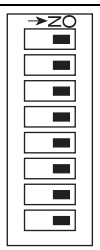
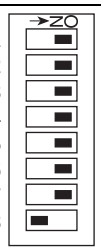
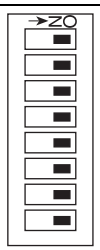
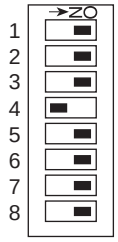
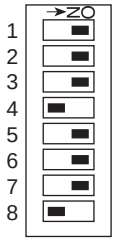
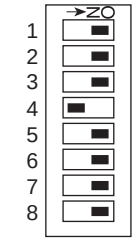
	JP6	JP7	JP8	SW2
All Reticon (RET)				
All Kodak & all Hamamatsu				
PI 1100 & 1752 devices **Note:** CCD selection in software hardware setup must match jumper settings.			 **8 phase**  **6 phase**	
All Thomson (THX)				

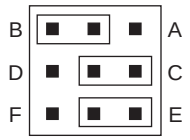
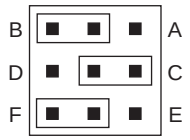
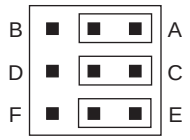
Table 6. SW3 position.

	25, 50 & 100 kHz	150 kHz	200 kHz
SITe front illuminated, PI front illuminated (except 1340)			
SITe back illuminated, PI back illuminated (except 1340)			
EEV 3 phase (except some 1024×256)			
All Reticon			
All Kodak & all Hamamatsu			
All Thomson			

	25, 50 & 100 kHz	150 kHz	200 kHz
EEV 6 phase 1024×256 & PI 1340 devices			

Shutter Closing Compensation Time

7. JP9 Shutter closing compensation time selector. See table below for proper setting.

All 576 × 384, 768 × 512, 1317 × 1035; all entrance slit shutters	
All other shutters	
ICCD	

Zero Offset

8. OFFSET This potentiometer sets the zero offset of the signal from the CCD before it is digitized. If, for example, the baseline of the detector appears high, this pot can be adjusted.

Other Jumpers

9. JP5, JP3 & some jumpers on the analog (half-size) board. These jumpers also set the A/D bits and the speed, but for the most part, they are clearly marked. The number of bits is factory set to match the A/D installed in the system and should never need changing. The A/D speed can be changed by the user, but not all speeds are possible for all devices.

Note: The 1024EHR and 1024EHRB devices can only be operated at a speed of 50 kHz with an ST-130 or ST-135 Controller.

Appendix C

GPIB Configuration

The National Instruments AT-GPIB/TNT Interface board is supplied with a configuration program, IBCONF. Once the board and program have been installed per the National Instruments documentation, the board must be configured from the Microsoft Windows 3.11 Control Panel for proper operation. A table of suggested configuration settings follows. Setting requirements may vary in some systems.

Headings	Selection Fields	Additional Information
Board Type	AT-GPIB/TNT	Board type selection is critical.
	0×120	Base I/O Address. Make selection match pattern shown in graphic.
	[7]	Interrupt Level
	[7]	DMA Channel
	[X]	Use demand mode DMA.
	500 ns	Bus Timing
	disabled	Cable length for high speed
Software **(click on button)**		
GPIB Address Section	Primary 0; Secondary: none	
	[NO]	Terminate read on EOS.
	[NO]	Set EOI with EOS on write.
	[NO]	8 bit EOS compare
	[X]	Send EOI @ end of write.
	0	EOS Byte
Advanced Section		
	[X]	System Controller
	10 sec	I/O time out (shorten if desired)
	Default	Parallel Poll Duration
	[NO]	Enable auto serial polling.
	[NO]	Enable C/C protocol.
	[X]	Assert REN when SC.

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Appendix D
GPIB Switch Settings

There are two DIP switch assemblies, with eight switches each, located just behind the front panel on the lower circuit board of the ST-135. They can be easily accessed without removing the upper boards.

These switches have two purposes. Switch Assembly 1 specifies the CCD chip type and the Controller type. Switch Assembly 2 specifies the GPIB address. Printed labels on the circuit board adjacent to the switches identifies them as SW1 (Switch 1) and SW2 (Switch 2). This appendix describes the required switch settings.

Figure 33. Switch Assembly 1

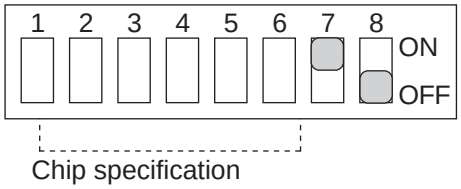
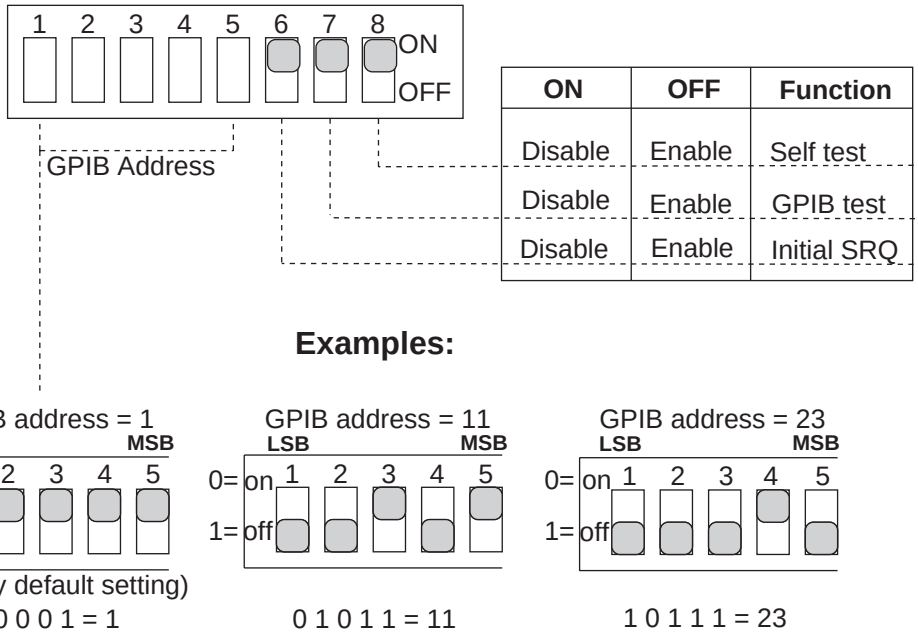


Figure 34. Switch Assembly 2



ON	OFF	Function
Disable	Enable	Self test
Disable	Enable	GPIB test
Disable	Enable	Initial SRQ

Supported CCD Chips by ST135

GPIB PROM	ID #	Chip Maker	Line	Strip	Dmy Lines	Dmy Strips	GPIB bd. Dip Switch 1 Position					
							1	2	3	4	5	6
2.1	1	Thmsn	578	384	2,0	8,15	OFF	ON	ON	ON	ON	ON
	2	EEV	578	384	1,0	12,13	ON	OFF	ON	ON	ON	ON
	3	EEV	1152	298	1,0	22,22	OFF	OFF	ON	ON	ON	ON
	4	EEV	1152	1242	1,0	22,22	ON	ON	OFF	ON	ON	ON
	5	Tek (SITE)	512	512	1,0	50,0	OFF	ON	OFF	ON	ON	ON
	6	Tek (SITE)	1024	1024	1,0	50,50	ON	OFF	OFF	ON	ON	ON
4.0	7	Retcn	400	1200	1,0	51,2	OFF	OFF	OFF	ON	ON	ON
4.1	8	Retcn	1024	1024	1,0	51,2	ON	ON	ON	OFF	ON	ON
	9	EEV	256	1024	13,12	8.8	OFF	ON	ON	OFF	ON	ON
	10	Retcn	512	512	1,0	50,0	ON	OFF	ON	OFF	ON	ON
	11	Tek (SITE)	2048	2044	1,0	50,54	OFF	OFF	ON	OFF	ON	ON
	12	Retcn	2048	2044	1,0	16,20	ON	ON	OFF	OFF	ON	ON
	13	Kodak	2044	2033	2,2	25,7	OFF	ON	OFF	OFF	ON	ON
4.4	14	Kodak	768	512	4,4	14,14	ON	OFF	OFF	OFF	ON	ON
	15	Kodak	1024	1280	2,2	4,20	OFF	OFF	OFF	OFF	ON	ON
	16	Kodak	1035	1317	1,1	26,5	ON	ON	ON	ON	OFF	ON
	17	Kodak	2048	3072	4,4	16,12	OFF	ON	ON	ON	OFF	ON
	18	PI	330	1100	1,0	16,16	ON	OFF	ON	ON	OFF	ON
	19	PI	532	1752	1,0	23,23	OFF	OFF	ON	ON	OFF	ON
4.5	20	EEV	256	1024	1,0	8,8	ON	ON	OFF	ON	OFF	ON
	21	EEV	1152	770	1,0	22,22	OFF	ON	OFF	ON	OFF	ON
	22	Hama	64	1024	1,2	10,10	ON	OFF	OFF	ON	OFF	ON
	23	Hama	128	1024	1,2	10,10	OFF	OFF	OFF	ON	OFF	ON
	24	Hama	256	1024	1,2	10,10	ON	ON	ON	OFF	OFF	ON
	25	Kodak	1024	1536	4,4	14,14	OFF	ON	ON	OFF	OFF	ON
	26	SITE	800	2000	1,0	15,15	ON	OFF	ON	OFF	OFF	ON
	27	Tek (SITE)	512	512	1,0	15,0	OFF	OFF	ON	OFF	OFF	ON
	28	Tek (SITE)	1024	1024	1,0	16,16	ON	ON	OFF	OFF	OFF	ON
4.5.1	17	EEV	100	1340	1,0	8,8	OFF	ON	ON	ON	OFF	ON
	29	EEV	400	1340	1,0	8,8	OFF	ON	OFF	OFF	OFF	ON
	30	EEV	700	1340	1,0	8,8	ON	OFF	OFF	OFF	OFF	ON
	31	EEV	1300	1340	1,0	8,8	OFF	OFF	OFF	OFF	OFF	ON
	32	PID	800	1000	1,0	15,15	ON	ON	ON	ON	ON	OFF
	33	THM	256	1024	18,18	0,0	OFF	ON	ON	ON	ON	OFF
	34	THM	512	512	2,2	11,20	ON	OFF	ON	ON	ON	OFF

Notes:

1. Switch position 5 is included since version 4.4.
2. Switch position 6 is included since version 4.5.
3. Entry 17 (KDK 1048 x 3072) was replaced by EEV 100 x 1340 since version 4.5.1.
4. Duplicate Entries (dimensionally the same but with different number of dummy pixels):

EEV	256 x 1024	#9	Original 3 and 6 phases; 13 pre and 12 post dummy strips.
		#20	8 phases and CCD 30; 1 pre and 0 post dummy strips.
TEK (SITE)	512 x 512	#5	Original; 50 pre and 0 post for #5 dummy strips. 27 µm pixels.
		#27	TEK 512x512D chips (back and front); 15 pre and 0 post dummy strips.
TEK (SITE)	1024 x 1024	#6	Original; 50 pre and 50 post dummy strips.
		#28	TEK 1024x1024D chips (back and front); 16 pre and 16 dummy strips.

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Appendix E
J5 Data Port Configuration

The J5 data port, located on the rear panel of the controller, can be used for digital I/O. Figure 35 and the pin configuration listing both appear below.

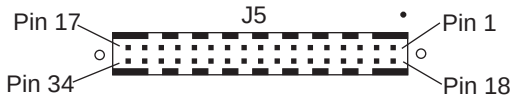

Figure 35. JP5 data port pin configuration

1		18	
2		19	
3	DIG GND	20	DIG GND
4	DATA IN 7	21	DATA IN 6
5	DATA IN 5	22	DATA IN 4
6	DATA IN 3	23	DATA IN 2
7	DATA IN 1	24	DATA IN 0
8	DIG GND	25	DIG GND
9		26	
10	DATA OUT 3	27	DATA OUT 2
11	DATA OUT 1	28	DATA OUT 0
12		29	
13	DIG GND	30	DIG GND
14	DATA OUT 4*	31	DATA OUT 4 RTN
15	DATA OUT 5*	32	DATA OUT 5 RTN
16	DATA OUT 6*	33	DATA OUT 6 RTN
17	DATA OUT 7*	34	DATA OUT 7 RTN

The "*" above denotes negative assertion. These upper 4 bits work as FET switches (maximum 60 V, 0.5 A). See the suggested test schematic in Figure 36.

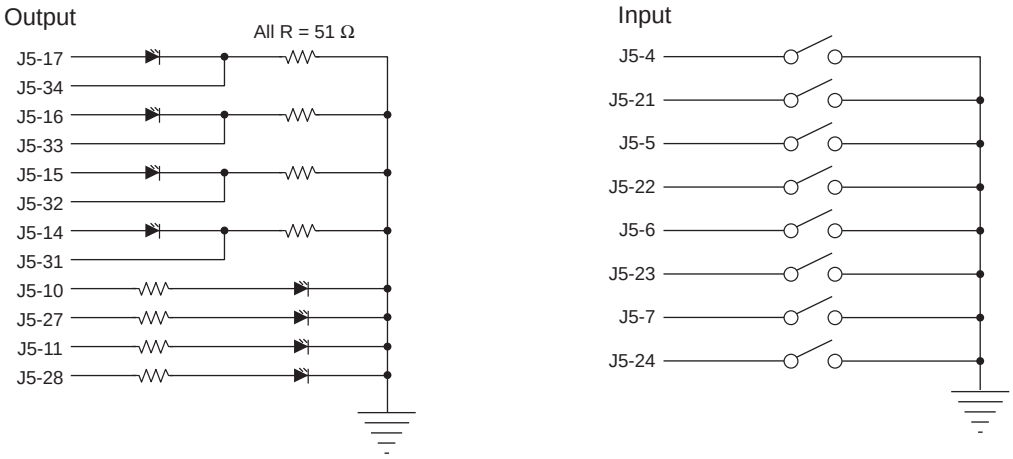

Figure 36. Suggested test schematic for J5 data port

Warranty & Service

Warranty

This equipment is warranted to be free from defects of material and workmanship. It is sold subject to the mutual agreement that the liability of RS Princeton Instruments, is limited to replacing defective parts and/or repairing malfunctioning equipment at its factory, provided the equipment is returned, transportation prepaid, within twelve (12) months of its factory ship date.

The purchaser agrees that RS Princeton Instruments shall assume no liability for consequential damages resulting from its use or from packaging of shipments returned to the factory.

Components which are damaged by misuse are not warranted. Units which have been modified by a customer are not warranted.

UV coatings are not covered by this warranty.

Equipment Repairs

It is recommended that units requiring service in the United States be returned to the factory located in Trenton, New Jersey. Before instrumentation is returned for service, please consult a service engineer at the factory. In many cases, the problem may be cleared up over the telephone.

If the unit needs to be returned, the service engineer will ask for a detailed explanation of the problems encountered and a purchase order to cover any charges. You will then receive a Returned Materials Authorization (RMA) number. Place this number on the package so the returned equipment can be easily identified when received at the factory. You must also include with the equipment a completed RMA form explaining the symptoms or problems encountered. Without this document, repair turnaround time will be considerably longer.

If the unit is under warranty, the customer is only responsible for the transportation and insurance charges to RS Princeton Instruments. RS Princeton Instruments is responsible for the return transportation charges. If the unit is out of warranty, the customer is responsible for all transportation charges (including insurance and duty fees, when applicable) as well as all charges incurred to perform the repairs. In this case, the customer can decide the insurance value.

International customers should contact your local manufacturers representative or distributor for repair information. *See next page for contact information.*

Contact Information

RS Princeton Instrument's manufacturing facility is located at the following address:

RS Princeton Instruments
3660 Quakerbridge Road
Trenton, NJ 08619 (USA)

Tel: 609-587-9797
Fax: 609-587-1970

Tech Support E-mail: techsupport@roperscientific.com

For technical support and service outside the United States, see our web page at www.roperscientific.com. An up-to-date list of addresses, telephone numbers, and e-mail addresses of RS Princeton Instrument's overseas offices and representatives is maintained on the web page.

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